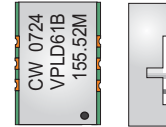


CRYSTAL CONTROLLED OSCILLATORS

3.3V SURFACE MOUNT VCXO OSCILLATOR



ABSOLUTE MAXIMUM RATINGS

TABLE 1.0

PARAMETER	UNITS	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Storage Temperature		-55	-	125	°C	
Supply Voltage	(Vcc)	-0.5	-	7.0	Vdc	
Control Voltage	(Vc)	-0.5	-	Vcc+0.5	Vdc	

OPERATING SPECIFICATIONS

TABLE 2.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Center Frequency	(Fo)	60	-	200	MHz	
Frequency Stability		-25	-	25	ppm	1
Frequency vs. Aging (10 Years)		-10	-	10	ppm	
Total Frequency Tolerance		-35	-	35	ppm	2
Operating Temperature Range		-40	-	85	°C	
Supply Voltage	(Vcc)	3.135	3.3	3.465	Vdc	
Supply Current	(Icc)	-	-	80	mA	
Period Jitter		-	2	5	ps rms	
Integrated Phase Jitter (BW=12kHz to 20MHz)		-	0.5	1	ps rms	
SSB Phase Noise at 10Hz offset		-	-60	-	dBc/Hz	
SSB Phase Noise at 100Hz offset		-	-90	-	dBc/Hz	
SSB Phase Noise at 1KHz offset		-	-120	-	dBc/Hz	
SSB Phase Noise at 10KHz offset		-	-140	-	dBc/Hz	
SSB Phase Noise at 100KHz offset		-	-145	-	dBc/Hz	

INPUT CHARACTERISTICS

TABLE 3.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
Control Voltage Range	(Vc)	0.3	1.65	3.0	Vdc	
Frequency Pullability		+/-75	-	+/-175		3
Absolute Pull Range (APR)		+/-30	-	-	ppm	4
Monotonic Linearity		-10	-	10	%	
Input Impedance		-	50K	-	Ohm	
Modulation Bandwidth (3dB)		10	-	-	KHz	
Enable Input Voltage (Low)	(Vil)	-	-	1.68	Vdc	5
Disable Input Voltage (High)	(Vih)	2.275	-	-	Vdc	5

LVPECL OUTPUT CHARACTERISTICS

TABLE 4.0

PARAMETER		MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
LOAD		-	-	50	Ohms	6
Voltage (High)	(Voh)	2.275	-	-	Vdc	
(Low)	(Vol)	-	-	1.68	Vdc	
Duty Cycle at 50% Level		45	50	55	%	
Rise / Fall Time 20% to 80%		-	-	1.0	ns	

PACKAGE CHARACTERISTICS

TABLE 5.0

Package	Non-hermetic package consisting of an FR4 substrate with grounded metal cover.
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PROCESS RECOMMENDATIONS

TABLE 6.0

Soldering Process	See the solder profile page 2.
Wash	Ultrasonic cleaning is not recommended.

VPLD61B

DESCRIPTION

The Connor-Winfield VPLD61B is a 3.3V Voltage Controlled Crystal Oscillator (VCXO) with Differential LVPECL outputs and Enable/Disable function. The VPLD61B is designed for use with PLL systems in SONET/SDH systems requiring low jitter and tight stability. No multiplication schemes are used in this oscillator design.

FEATURES

- SURFACE MOUNT PACKAGE
- 3.3V OPERATION
- LOW JITTER <1ps RMS
- FREQUENCY STABILITY: ±25ppm
- TEMPERATURE RANGE: -40 to 85°C
- DIFFERENTIAL LVPECL OUTPUTS
- ENABLE / DISABLE FUNCTION
- TAPE AND REEL PACKAGING MEETS EIA-481A STANDARD
- RoHS COMPLIANT / LEAD FREE

ORDERING INFORMATION

VPLD61B - 155.52M

VCXO SERIES CENTER FREQUENCY

Specifications subject to change without notice.

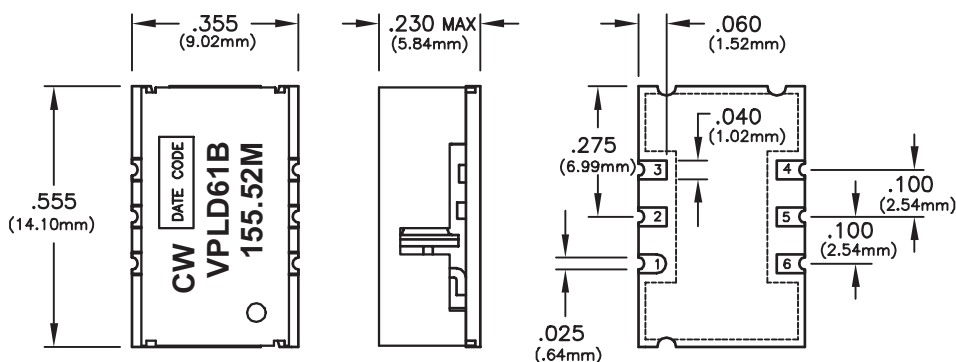


CRYSTAL CONTROLLED OSCILLATORS

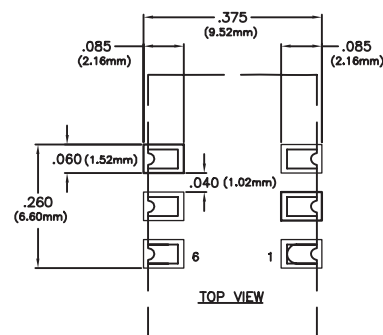
Notes

- 1.0 Frequency vs. change in temperature. Control Voltage @ 1.65V
- 2.0 Includes frequency vs. change in temperature, supply voltage and load variations, shock and vibration, and aging.
- 3.0 Referenced to Fo @ 25°C, Positive slope.
- 4.0 Absolute pull range (APR) is the minimum guaranteed pull range of the VCXO under all conditions over lifetime operation. The APR is referenced to Fo. Positive Slope.
- 5.0 Outputs are enabled with no connection on pad 2. When oscillator is disabled the true output is in a low state (VoI) and the complementary output is in the high state (VoH)
- 6.0 Output terminated into 50 ohms into Vcc – 2.0Vdc or Thevenin equivalent.

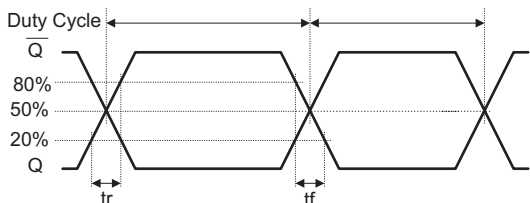
Package Outline



Suggested Pad Layout



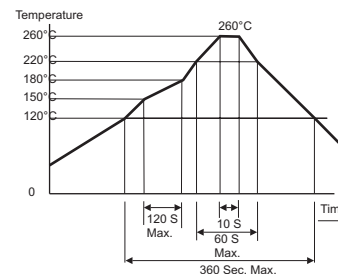
Output Waveform



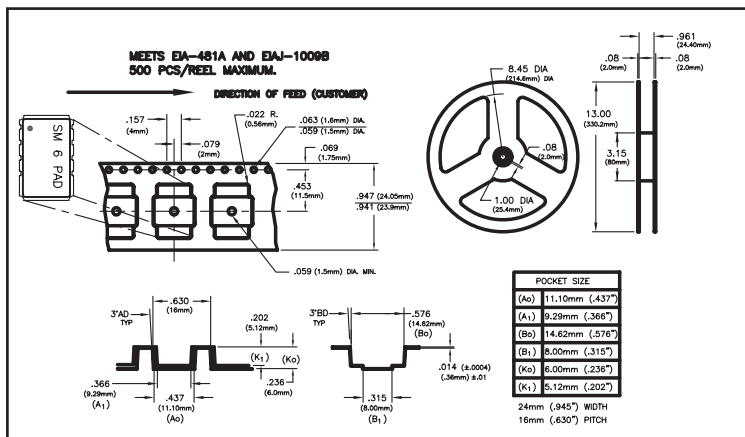
Pad Connections

Pad	Function
1	Control Voltage
2	Enable / Disable
3	Ground (Case)
4	Output Q
5	Comp Output Q
6	Vcc

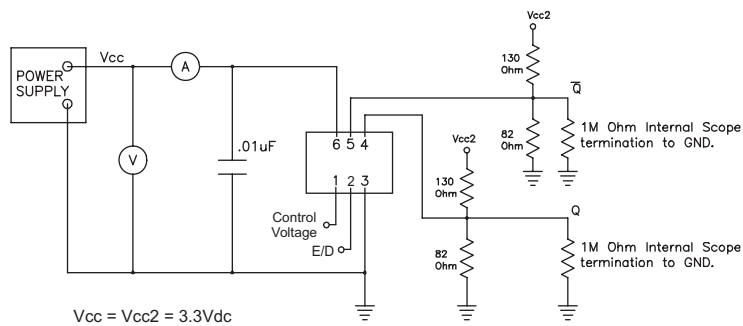
Solder Profile



Tape and Reel Information



Test Circuit



Specifications subject to change without notice.