Low Distortion, High Speed Rail-to-Rail Input/Output Amplifier

Known Good Die

AD8065-KGD-CHIP

FEATURES

FET input amplifier
1 pA input bias current
Low cost
High speed: 145 MHz, −3 dB bandwidth (G = +1)
180 V/µs slew rate (G = +2)
Low noise
  7 nV/√Hz (f = 10 kHz)
  0.6 fA/√Hz (f = 10 kHz)
Wide supply voltage range: 5 V to 24 V
Single-supply and rail-to-rail output
Low offset voltage 1.5 mV maximum
High common-mode rejection ratio: −100 dB
SFDR −88 dBc @ 1 MHz
Low power: 6.4 mA/amplifier typical supply current
Known good die (KGD): these die are fully guaranteed to data sheet specifications

APPLICATIONS

Photodiode preamps
Filters
A/D drivers
Level shifting
Buffering

GENERAL DESCRIPTION

The AD8065-KGD-CHIP *FastFET*™ amplifier is a voltage feedback amplifier with a FET input offering high performance and ease of use. With a wide supply voltage range from 5 V to 24 V, and the ability to operate on single supplies, with a bandwidth of 145 MHz, the AD8065-KGD-CHIP is designed to work in a variety of applications. For added versatility, the amplifier also features a rail-to-rail output.

Despite the low cost, the amplifiers provide excellent overall performance. The differential gain and phase errors of 0.02% and 0.02°, respectively, along with 0.1 dB flatness out to 7 MHz, make these amplifiers ideal for video applications. Additionally, they offer a high slew rate of 180 V/µs, excellent distortion (SFDR of −88 dBc at 1 MHz), extremely high common-mode rejection of −100 dB, and a low input offset voltage of 1.5 mV maximum under warmed up conditions. The AD8065-KGD-CHIP operates using only a 6.4 mA/amplifier typical supply current and are capable of delivering up to 30 mA of load current.

The AD8065-KGD-CHIP is rated to work over the industrial temperature range of −40°C to +85°C.

Additional application and technical information can be found in the AD8065 data sheet.

[1]Protected by U.S. patent numbers 6,486,737B1; 6,518,842B1

Rev. 0 **Document Feedback**

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REVISION HISTORY

10/12—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±5 V at T_A = 30°C, R_L = 1 kΩ to midsupply, G = 1, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Status	Unit
DYNAMIC PERFORMANCE						
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p	100	145		GBD[1]	MHz
	G = +2, V_O = 0.2 V p-p		50			MHz
	G = +2, V_O = 2 V p-p		42			MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		7			MHz
Input Overdrive Recovery Time	G = +1, −5.5 V to +5.5 V		175			ns
Output Recovery Time	G = −1, −5.5 V to +5.5 V		170			ns
Slew Rate	G = +2, V_O = 4 V step	130	180		GBD[1]	V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		55			ns
	G = +2, V_O = 8 V step		205			ns
NOISE/HARMONIC PERFORMANCE						
SFDR	f_C = 1 MHz, G = +2, V_O = 2 V p-p		−88			dBc
	f_C = 5 MHz, G = +2, V_O = 2 V p-p		−67			dBc
	f_C = 1 MHz, G = +2, V_O = 8 V p-p		−73			dBc
Third-Order Intercept	f_C = 10 MHz, R_L = 100 Ω		24			dBm
Input Voltage Noise	f = 10 kHz		7			nV/√Hz
Input Current Noise	f = 10 kHz		0.6			fA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.02			%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.02			Degrees
DC PERFORMANCE						
Input Offset Voltage	V_{CM} = 0 V		0.4	1.5	Tested	mV
Input Offset Voltage Drift			1	17	GBD[1]	µV/°C
Input Bias Current			2			pA
	T_{MIN} to T_{MAX}		25			pA
Input Offset Current			1			pA
	T_{MIN} to T_{MAX}		1			pA
Open-Loop Gain	V_O = ±3 V, R_L = 1 kΩ	100	113		Tested	dB
INPUT CHARACTERISTICS						
Common-Mode Input Impedance			1000 || 2.1			GΩ || pF
Differential Input Impedance			1000 || 4.5			GΩ || pF
Input Common-Mode Voltage Range						
FET Input Range		−5 to +1.7	−5.0 to +2.4		GBD[1]	V
Common-Mode Rejection Ratio	V_{CM} = −1 V to +1 V	−85	−100		Tested	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 1 kΩ	−4.88 to +4.9	−4.94 to +4.95		Tested	V
	R_L = 150 Ω		−4.8 to +4.7			V
Output Current	V_O = 9 V p-p, SFDR ≥ −60 dBc, f = 500 kHz		35			mA
Short-Circuit Current			90			mA
Capacitive Load Drive	30% overshoot G = +1		20			pF
POWER SUPPLY						
Operating Range		5		24	Tested	V
Quiescent Current per Amplifier			6.4	7.2	Tested	mA
Power Supply Rejection Ratio	V_S ± 2 V	−85	−100		Tested	dB

[1] GBD = Guaranteed By Design.

V_S = ±12 V at T_A = 30°C, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Status	Unit
DYNAMIC PERFORMANCE						
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p	100	145		GBD[1]	MHz
Slew Rate	G = +2, V_O = 4 V step	130	180		GBD[1]	V/µs
DC PERFORMANCE						
Input Offset Voltage	V_{CM} = 0 V		0.4	1.5	Tested	mV
Input Offset Voltage Drift			1	17	GBD[1]	µV/°C
Input Bias Current			3			pA
Input Offset Current			2			pA
Open-Loop Gain	V_O = ±10 V	103	114		Tested	dB
INPUT CHARACTERISTICS						
Input Common-Mode Voltage Range						
FET Input Range		−12 to +8.5	−12.0 to +9.5		GBD[1]	V
Common-Mode Rejection Ratio	V_{CM} = −1 V to +1 V	−85	−100		Tested	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 1 kΩ	−11.8 to +11.8	−11.9 to +11.9		Tested	V
POWER SUPPLY						
Power Supply Rejection Ratio	V_S ± 2 V	−84	−93		Tested	dB
Quiescent Current per Amplifier			6.6	7.4	Tested	mA

[1] GBD = Guaranteed By Design.

V_S = +5 V at T_A = 30°C, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Status	Unit
DYNAMIC PERFORMANCE						
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p	125	155		GBD[1]	MHz
Slew Rate	G = +2, V_O = 2 V step	105	160		GBD[1]	V/µs
DC PERFORMANCE						
Input Offset Voltage	V_{CM} = 1.0 V		0.4	1.5	Tested	mV
Input Offset Voltage Drift			1	17	GBD[1]	µV/°C
Input Bias Current			1			pA
Input Offset Current			1			pA
Open-Loop Gain	V_O = 1 V to 4 V	100	113		Tested	dB
INPUT CHARACTERISTICS						
Input Common-Mode Voltage Range						
FET Input Range		0 to 1.7	0 to 2.4		GBD[1]	V
Common-Mode Rejection Ratio	V_{CM} = 1 V to 2 V	−78	−91		Tested	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 1 kΩ	0.1 to 4.85	0.03 to 4.95		Tested	V
POWER SUPPLY						
Power Supply Rejection Ratio	V_S ± 2 V	−78	−100		Tested	dB
Quiescent Current per Amplifier			6.4	7.0	Tested	mA

[1] GBD = Guaranteed by Design.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	26.4 V
Common-Mode Input Voltage	V_{EE} − 0.5 V to V_{CC} + 0.5 V
Differential Input Voltage	±1.8 V
Storage Temperature	−65°C to +125°C
Operating Temperature Range	−40°C to +105°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PAD CONFIGURATION AND FUNCTION DESCRIPTIONS

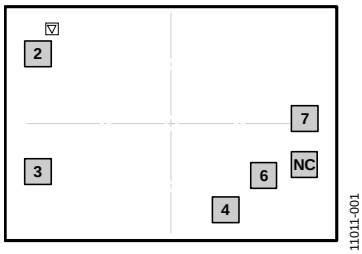

Figure 1. AD8065 Die Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	X-Axis	Y-Axis	Mnemonic	Description
2	−485	254	−IN	Inverting Input.
3	−485	−172	+IN	Noninverting Input.
4	201	−301	$-V_S$	Negative Supply.
6	343	−189	V_{OUT}	Output.
7	485	25	$+V_S$	Positive Supply.

OUTLINE DIMENSIONS

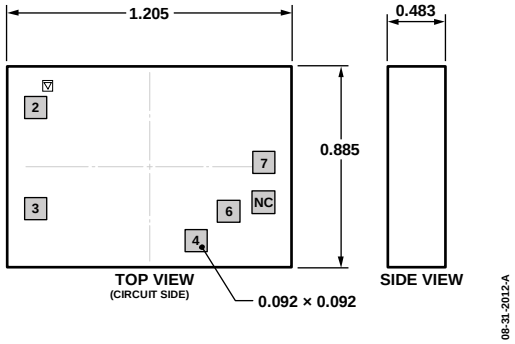

Figure 2. 6-Pad Bare Die [CHIP]
(C-6-5)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Typical Die Specifications

Parameter	Value	Unit
Chip Size	1205 × 855	µm
Die Size	47.4 × 33.7	Mil
Thickness	483	µm
Bond Pads (Min Size)	92 × 92	µm
Bond Pad Composition	1% Copper Doped Aluminum	%
Backside	Si	Not Applicable
Passivation	Doped oxide/SiN	Not Applicable
ESD	HBM 1000	V

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Ablestik 84-1LMIS R4
Bonding Method	1 mil gold

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8065-KGD-CHIP	–40°C to +85°C	6-Pad Bare Die [CHIP]	C-6-5

NOTES