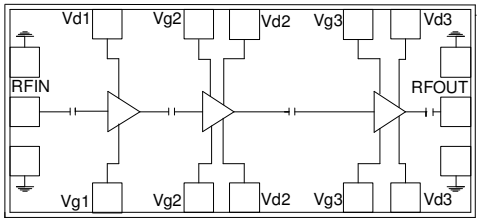
12.5 – 14.5 GHz 2 Watt Power Amplifier

Features

- **Frequency Range : 12.5 – 14.5GHz**
- **33 dBm output Psat**
- **25 dB Power gain**
- **27% PAE**
- **High IP3**
- **Input Return Loss > 8 dB**
- **Output Return Loss > 10 dB**
- **Dual bias operation**
- **No external matching required**
- **DC decoupled input and output**
- **0.5 µm InGaAs pHEMT Technology**
- **Chip dimension: 3.1 x 1.8 x 0.1 mm**

Functional Diagram



Typical Applications

- **RADAR**
- **MMDS**
- **VSAT**

Description

The ASTRA 2154041 is a three stage GaAs PHEMT Class AB Power Amplifier MMIC. The PA delivers output power of 33dBm with a small signal gain of 25dB and 27% PAE. The input/output are matched to 50 ohms and the circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Drain supply voltage (Vd)	+10	volts
Drain current (Idq)	1050	mA
RF input power (RFin at Vd=9V)	20	dBm
Operating temperature	-50 to +80	^{o}C
Storage Temperature	-65 to +150	^{o}C

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications [1] @ T_A = 25 °C, $V_{d1} = V_{d2}$ = 8V
$V_{g1} = V_{g2}$ = -0.85V Z_o =50 Ω

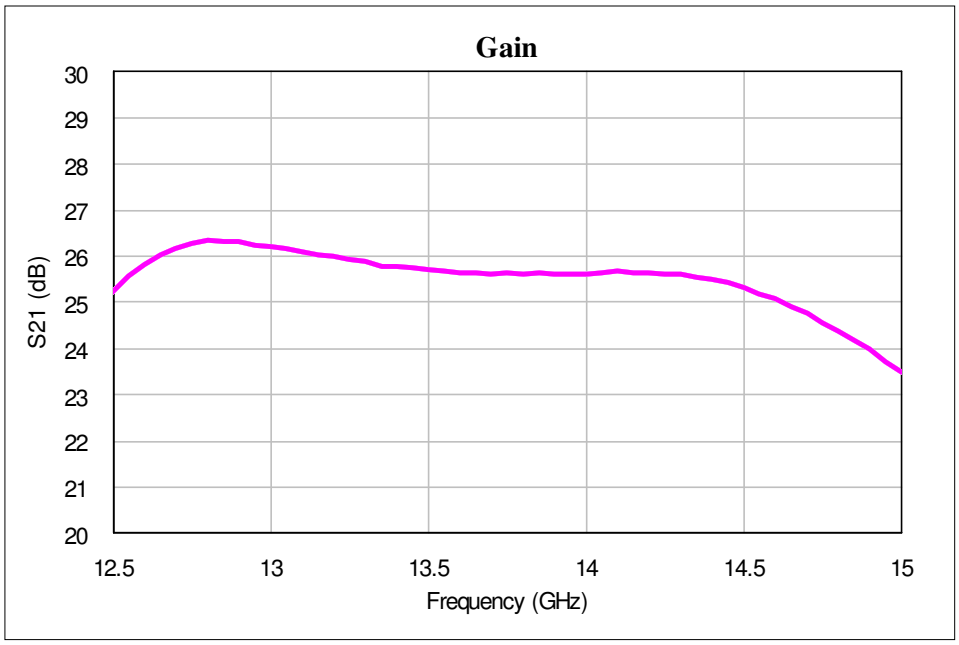
Parameter	Min.	Typ.	Max.	Units
Frequency Range	12.5		14.5	GHz
Gain	--	25	--	dB
Gain Flatness		+/- 0.5	--	dB
Input Return Loss	--	8	--	dB
Output Return Loss	--	10	--	dB
Output 1dB compression point (P1dB)	--	+32.5	--	dBm
Output Third Order Intercept point (OIP3)[1]	--	42	--	dBm
PAE [2]	--	27	--	%
Drain Bias Voltage (Vd1, Vd2)	-	8,8	10,10	V
Gate Bias Voltage (Vg1, Vg2)	-	-0.85,-0.85	-0.7,-0.7	V
Supply Current (I_{dq})	-	0.77	-	A
Supply Current (I_{dsat}[2])	-	0.84	-	A

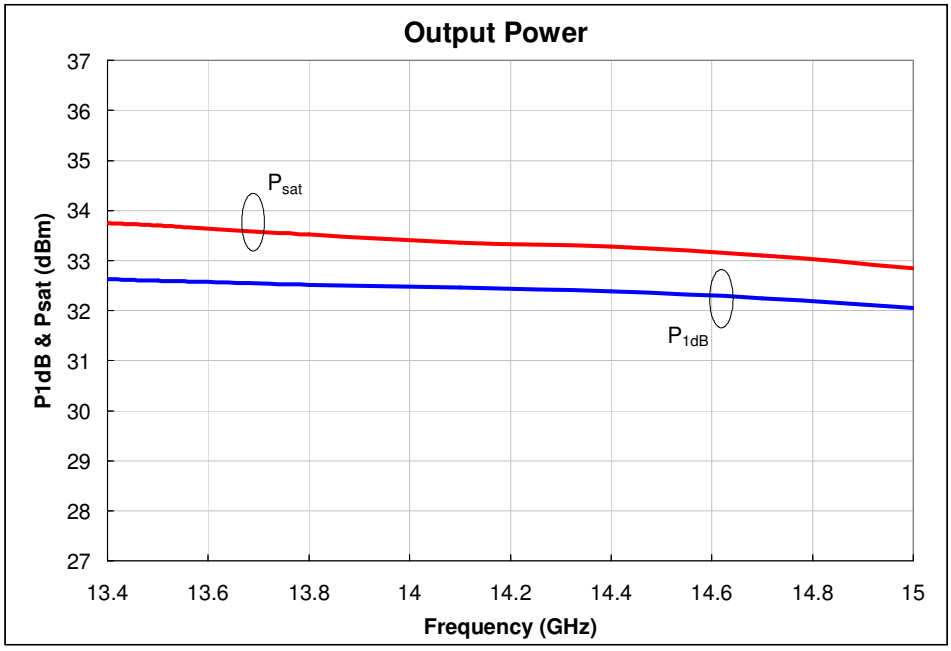
Note:

1. Measured at output 1dB compression point.
2. I_{dsat} is the maximum current under input RF drive condition.

Test fixture data

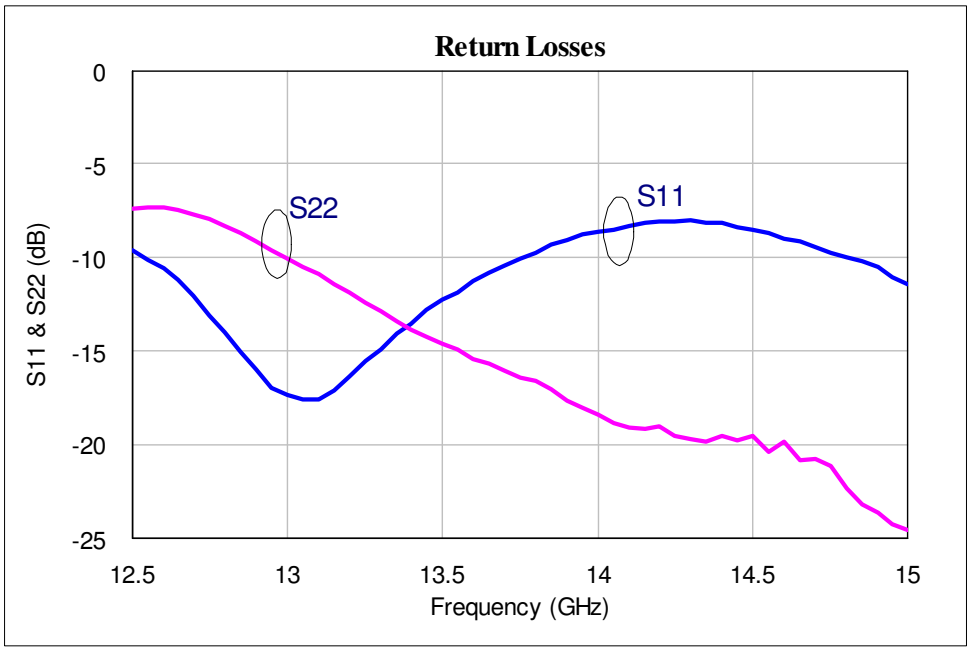
V_{d1} = V_{d2} = 8V, V_{g1} = V_{g2} = -0.85V, Idq =770mA, T_B = 40 °C

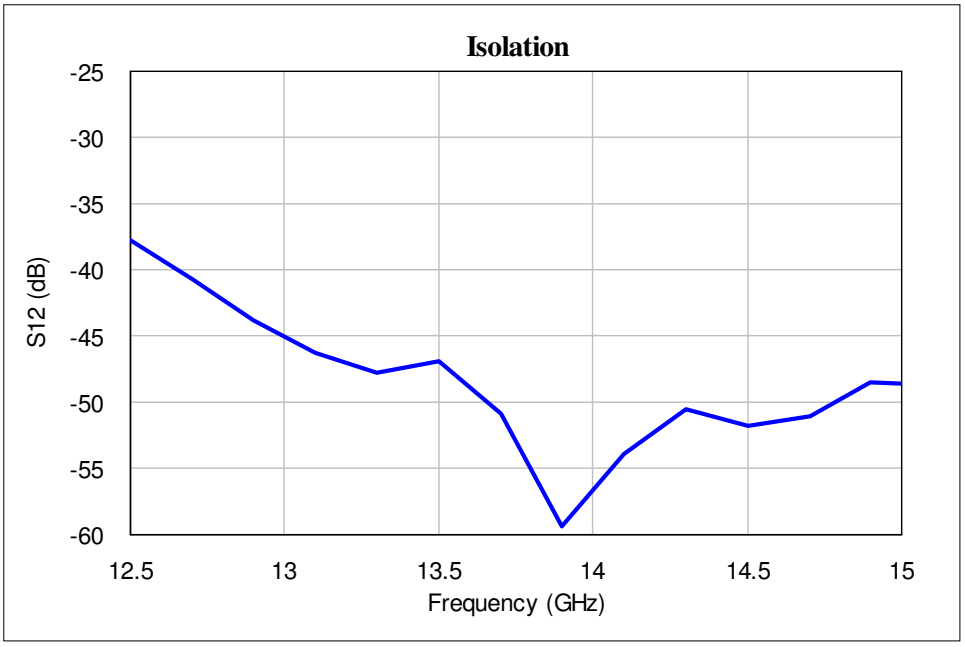




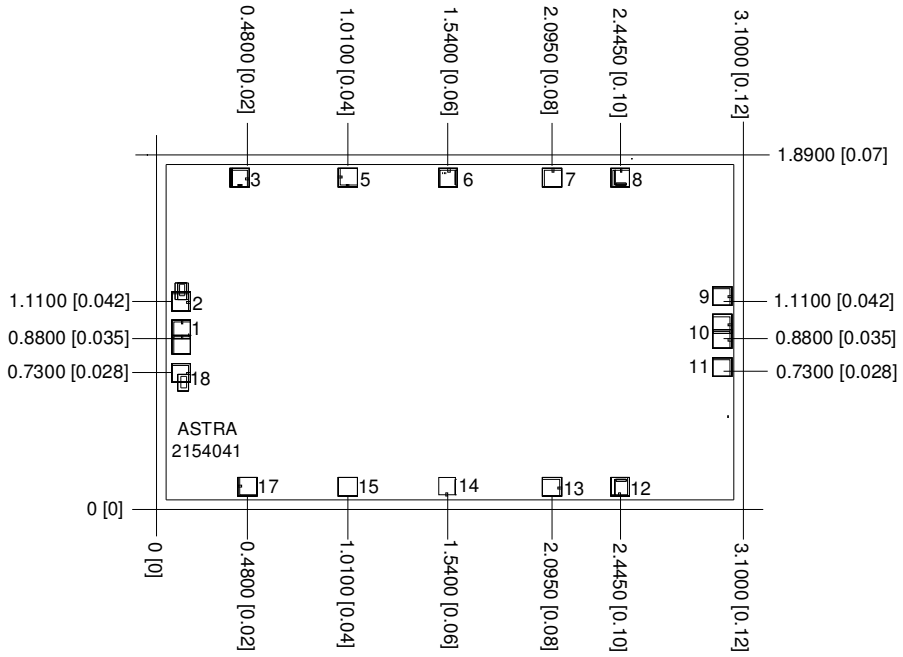
Test fixture data

V_{d1} = V_{d2} = 8V, V_{g1} = V_{g2} = -0.85V, Total Current =770mA, T_B = 40 °C





Mechanical Characteristics

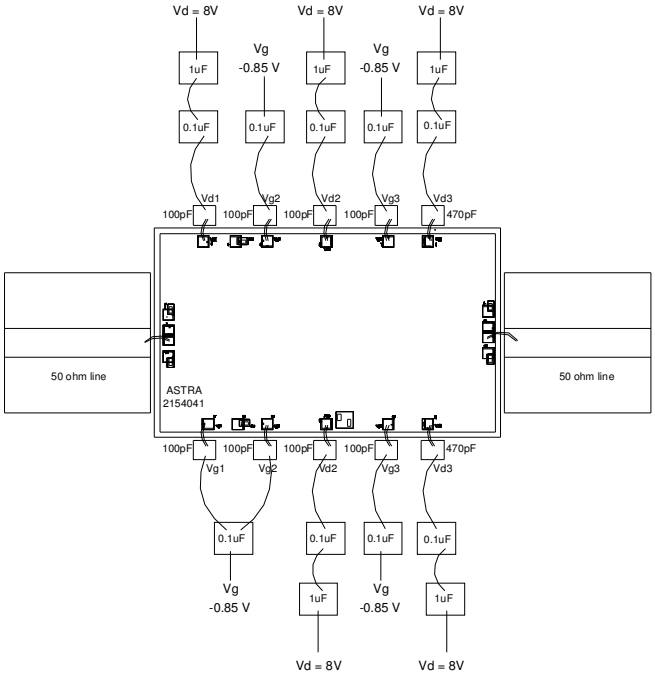


Units: millimeters (inches)

Note:

1. All RF and DC bond pads are 100µm x 100µm
2. Pad no. 1 : RF IN
3. Pad no. 17 : 1st stage gate voltage
4. Pad no. 3 : 1st stage drain voltage
5. Pad no. 5,15 : 2nd stage gate voltage
6. Pad no. 6,14 : 2nd stage drain voltage
7. Pad no. 7,13 : 3rd stage gate voltage
8. Pad no. 8,12 : 3rd stage drain voltage
9. Pad no. 10 : RF OUT

Recommended Assembly Diagram



Note :

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input, RF output and from chip bond pad to 100pF capacitor.
2. Input and output 50 ohm lines are on 5 mil RT Duroid substrate.
3. The bond numbers shown in assembly diagram are as per bond pad numbers printed on the die.
4. The RF input & output ports are DC decoupled on-chip.
5. Coefficient of thermal expansion matching is recommended for reliability purpose.
6. Use high thermal conductive material for die mounting for long term reliability.
7. Maintain base plate temperature less than 70 degC under RF operation for optimum performance.

Die attach: For Epoxy attachment, use of a two-component conductive epoxy is recommended. An epoxy fillet should be visible around the total die periphery. If Eutectic attachment is preferred, use of fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200µm length of wedge bonds is advised. Single Ball bonds of 250-300µm though acceptable, may cause a deviation in RF performance.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice