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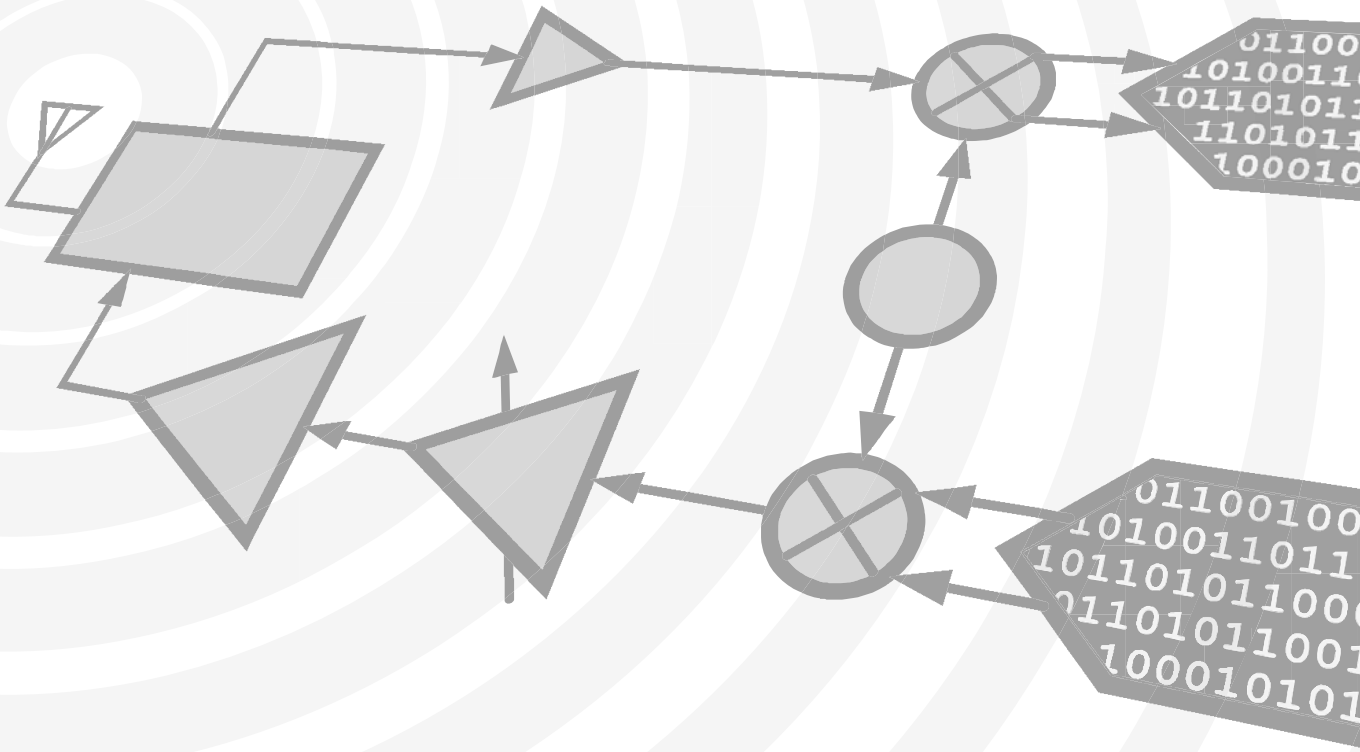

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v00.0813

HMC7357LP5GE

GaAs pHEMT MMIC 2 WATT POWER AMPLIFIER, 5.5 - 8.5 GHz

Typical Applications

The HMC7357LP5GE is ideal for:

- Point-to-Point Radios
- Point-to-Multi-Point Radios
- VSAT & SATCOM

Features

+35 dBm Pout @ 34% PAE

High P1dB Output Power: +34 dBm

High Output IP3: +41.5 dBm

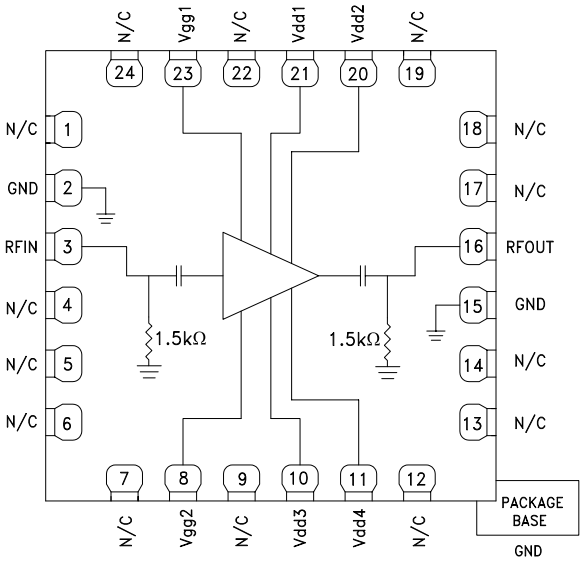
High Gain: 29 dB

50 Ohm Matched Input/Output

Supply Voltage: Vdd = +8V @ 1200 mA

24-Lead 5x5 mm SMT Package

Functional Diagram



General Description

The HMC7357LP5GE is a three-stage GaAs pHEMT MMIC Medium Power Amplifier that operates between 5.5 and 8.5 GHz. The amplifier provides 29 dB of gain and +35 dBm of saturated output power at 34% PAE from a +8V supply. With an excellent Output IP3 of +41.5 dBm, the HMC7357LP5GE is ideal for linear applications such as high capacity point-to-point and point-to-multi-point radios or VSAT/SATCOM applications demanding +35 dBm of efficient saturated output power. The RF I/Os are internally matched to 50 Ohms for ease of use. The HMC7357LP5GE is packaged in a leadless 5x5 mm plastic surface mount package and is compatible with surface mount manufacturing techniques.

Electrical Specifications, T_A = +25° C

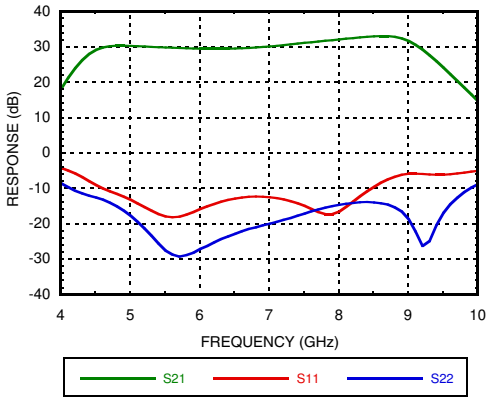
Vdd1 = Vdd2 = Vdd3 = Vdd4 = 8V, Idd = 1200 mA [1]

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		5.5 - 7			7 - 8.5		GHz
Gain	26.5	29.5		28	31		dB
Gain Variation Over Temperature		0.0214			0.0234		dB/ °C
Input Return Loss		14			14		dB
Output Return Loss		22			15		dB
Output Power for 1 dB Compression (P1dB)	31.5	34.5		31.5	34.5		dBm
Saturated Output Power (Psat)		35			35		dBm
Output Third Order Intercept (IP3)[2]		41.5			41.5		dBm
Total Supply Current (Idd)		1200			1200		mA

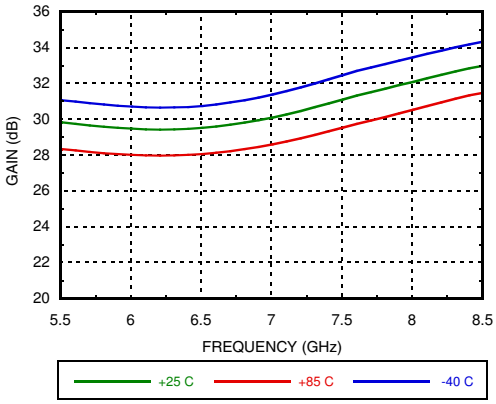
[1] Adjust Vgg between -2 to -0.4V to achieve Idd = 1200 mA typical.

[2] Measurement taken at +8V @ 1200 mA, Pout / Tone = +20 dBm

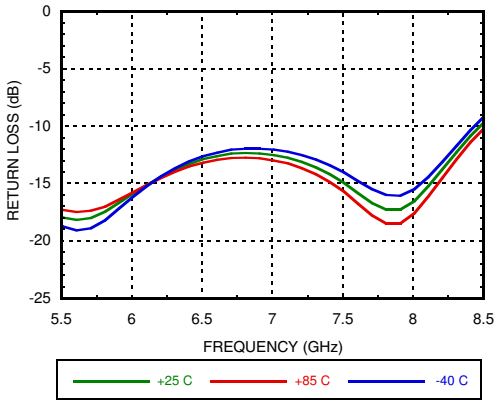
Gain & Return Loss



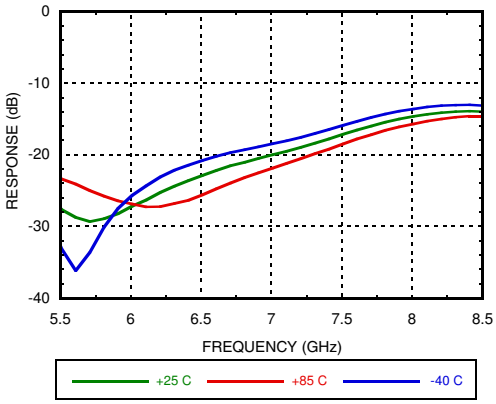
Gain vs. Temperature



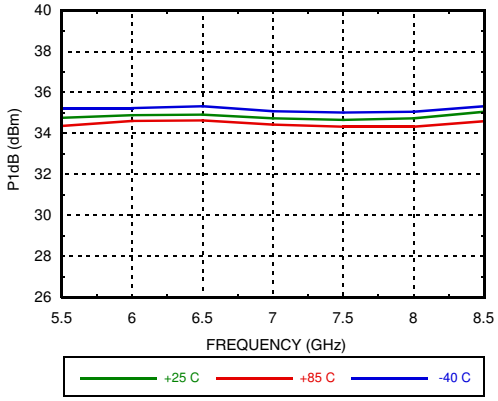
Input Return Loss vs. Temperature



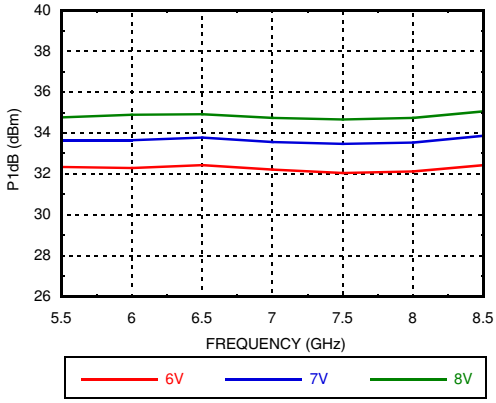
Output Return Loss vs. Temperature



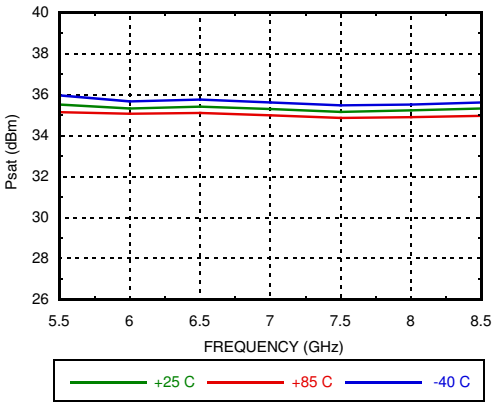
P1dB vs. Temperature



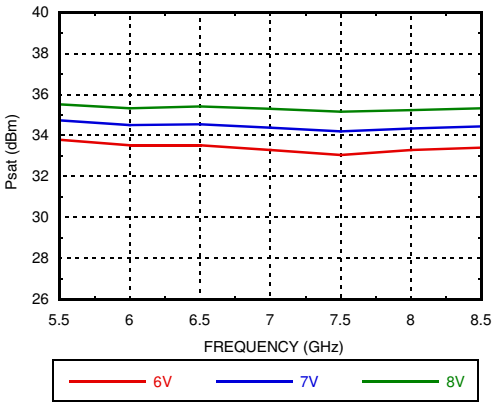
P1dB vs Supply Voltage



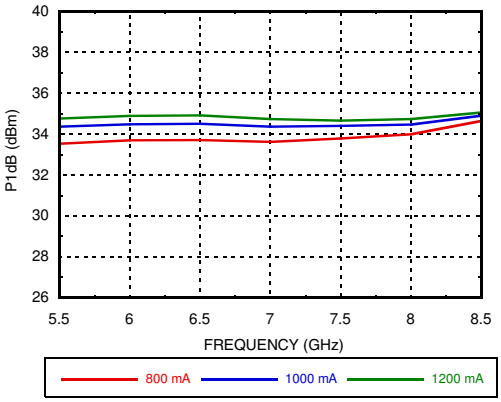
Psat vs. Temperature



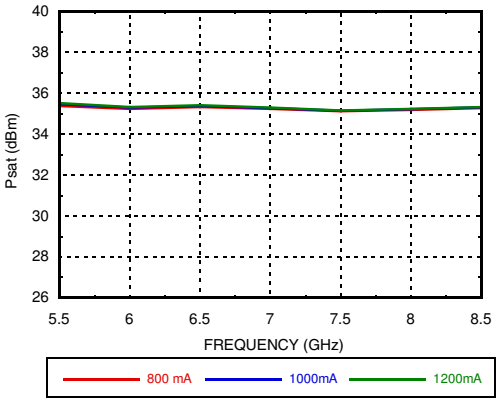
Psat vs. Supply Voltage



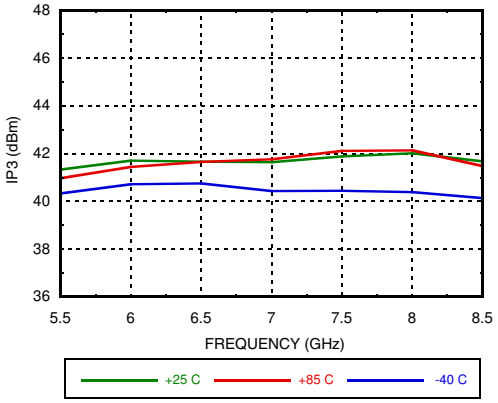
P1dB vs. Supply Current



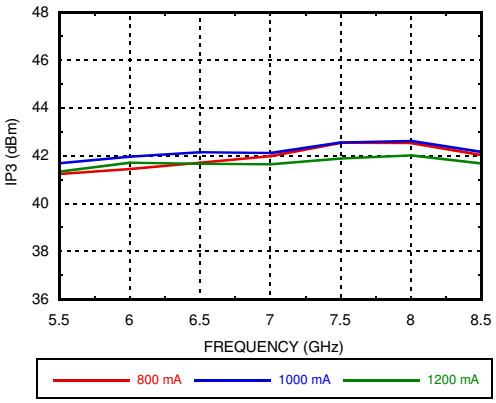
Psat vs. Supply Current



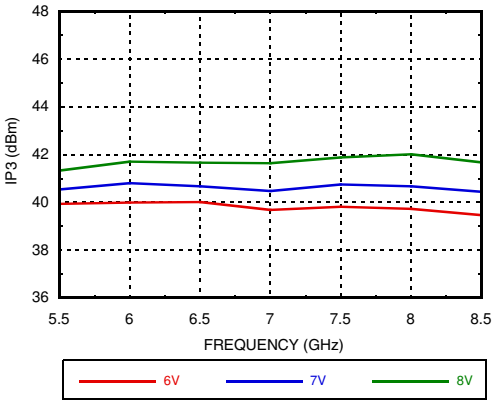
Output IP3 vs. Temperature, Pout/tone = +20 dBm



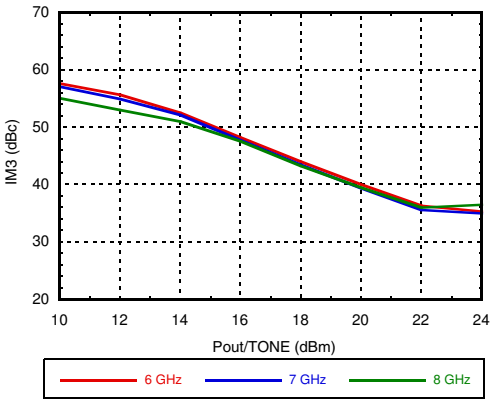
Output IP3 vs. Supply Current, Pout/tone = +20 dBm



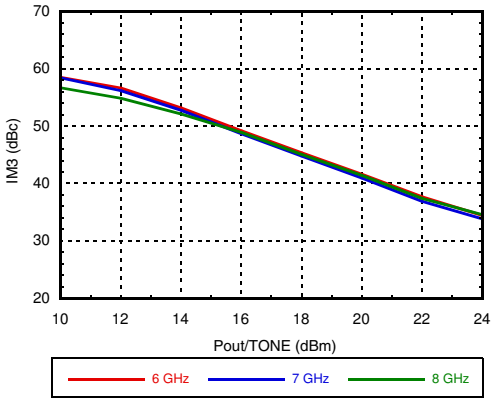
Output IP3 vs. Supply Voltage, Pout/tone = +20 dBm



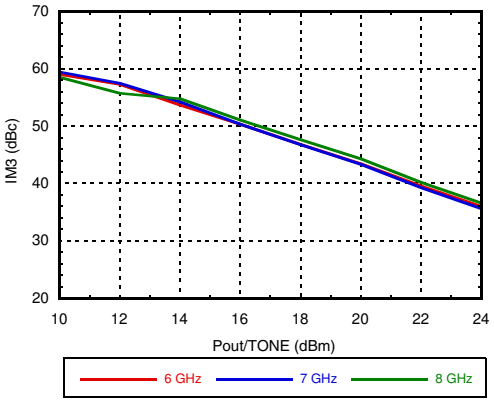
Output IM3 @ Vdd = +6V



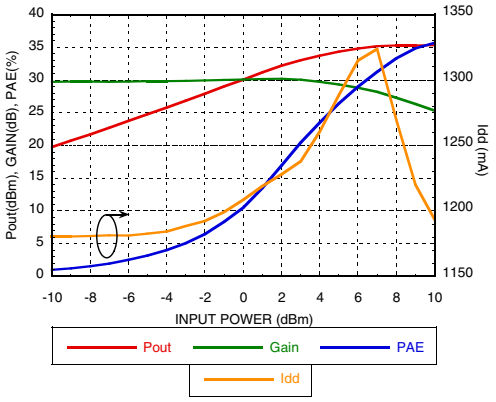
Output IM3 @ Vdd =+7V



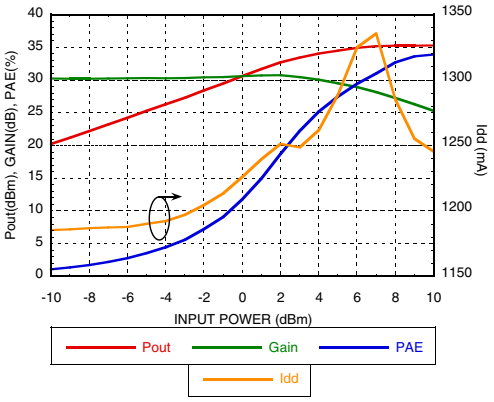
Output IM3 @ Vdd = +8V



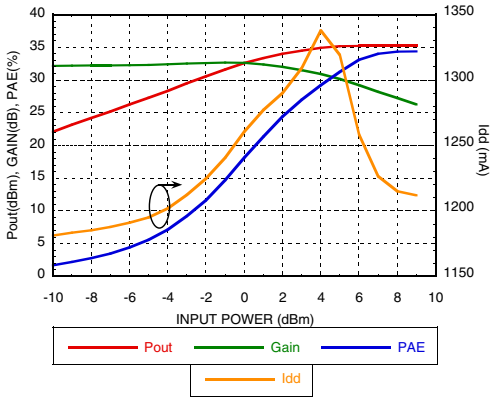
Power Compression @ 6 GHz



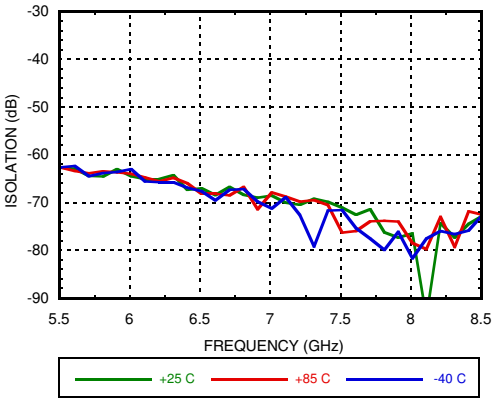
Power Compression @ 7 GHz



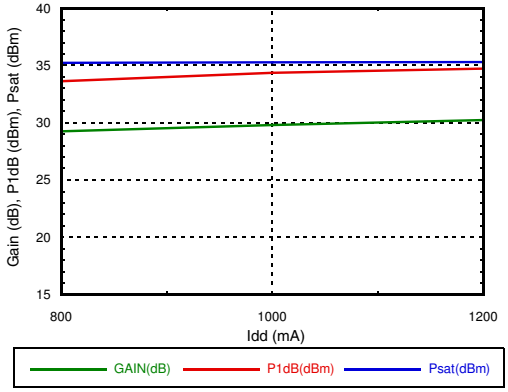
Power Compression @ 8 GHz



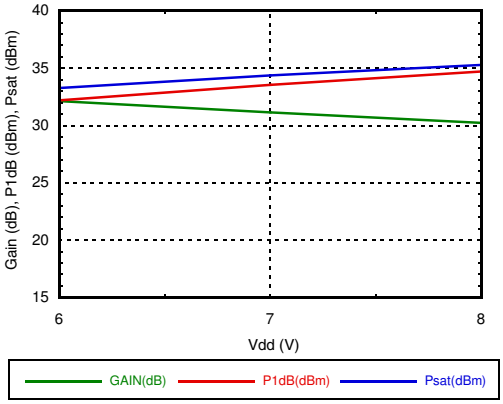
Reverse Isolation vs. Temperature



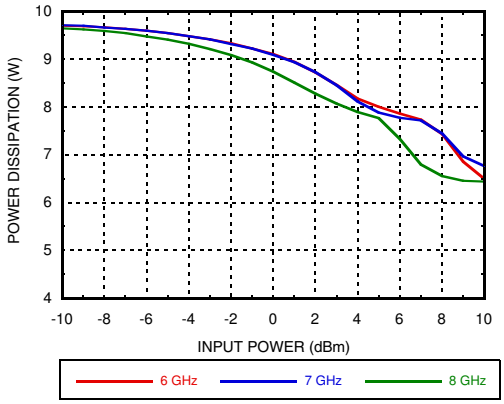
Gain & Power vs. Supply Current @ 7 GHz



Gain & Power vs. Supply Voltage @ 7 GHz



Power Dissipation



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Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+9 Vdc
Gate Bias Voltage (Vgg)	-2 to -0.4 Vdc
RF Input Power (RFIN)	+22 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 133mW/°C above 85 °C)	12.6 W
Thermal Resistance (channel to ground paddle)	7.5 °C/W
Storage Temperature	-65 to 150°C
Operating Temperature	-40 to 85 °C
ESD Sensitivity (HBM)	Class 1A, passed 250V

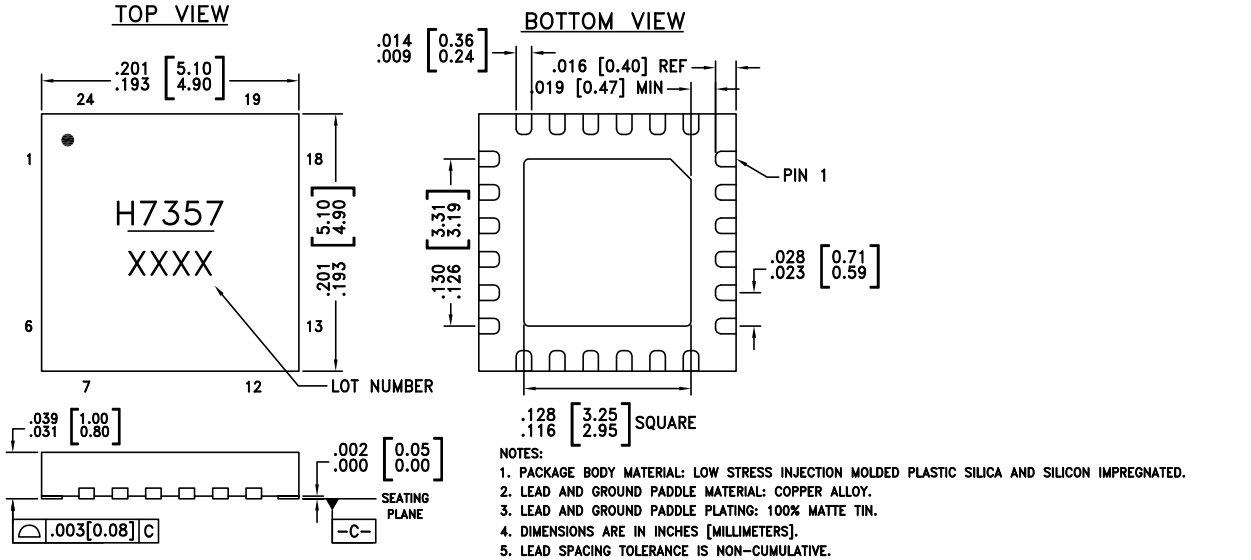
Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+6	1200
+7	1200
+8	1200

Adjust Vgg to achieve Idd = 1200 mA

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



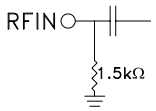
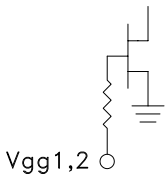
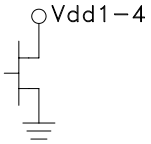
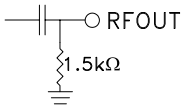
NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

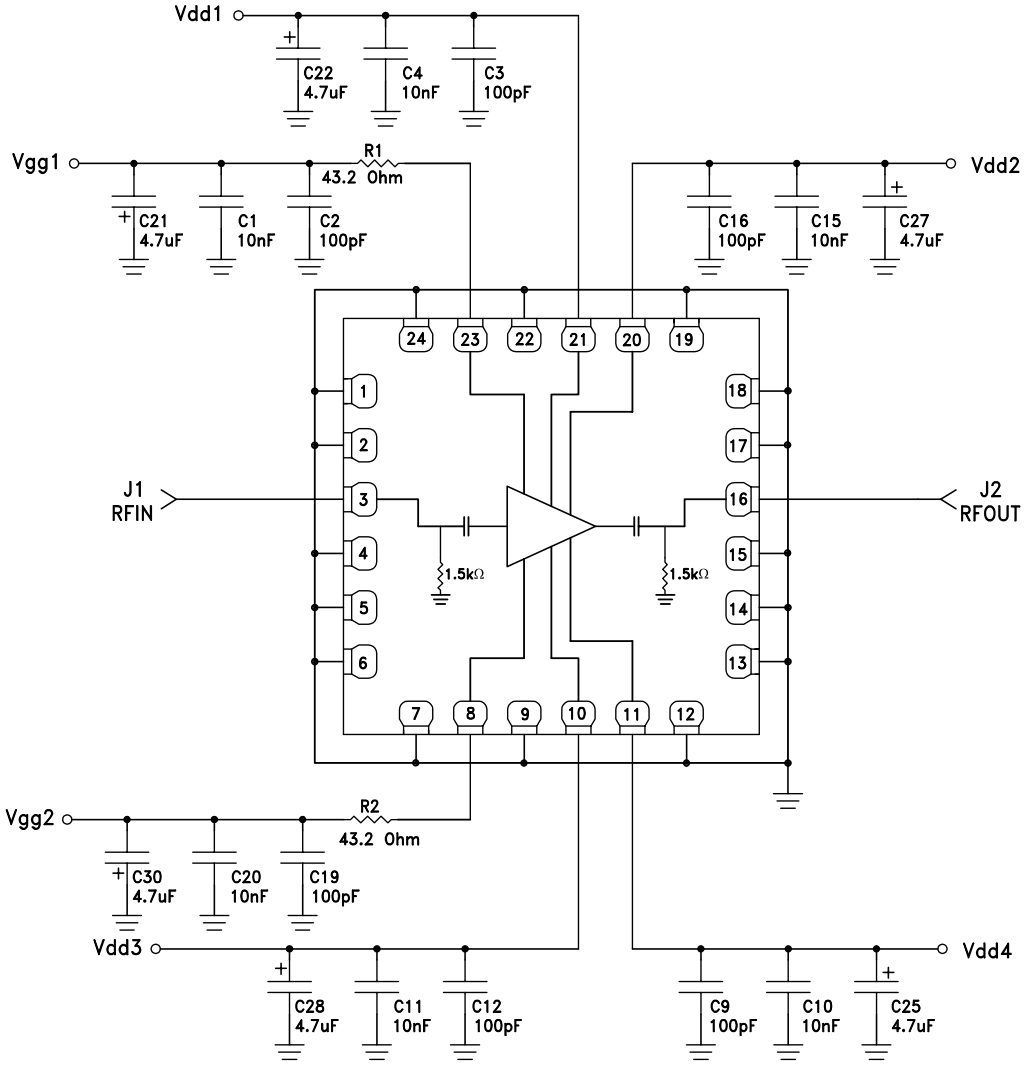
Part Number	Package Body Material	Lead Finish	MSL Rating [2]	Package Marking [1]
HMC7357LP5GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H7357 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

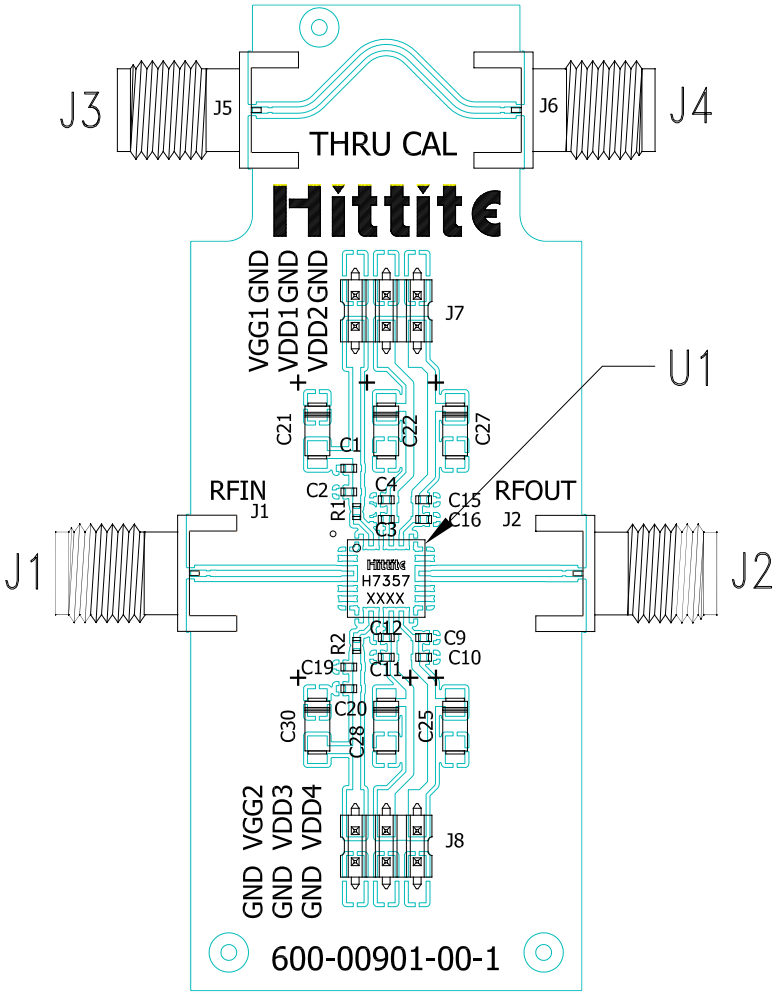
Pin Descriptions

Pad Number	Function	Description	Interface Schematic
1, 4, 5, 6, 7, 9, 12, 13, 14, 17, 18, 19, 22, 24	N/C	These pins are not connected internally; however all data shown herein was measured with these pins connected to RF/DC ground externally.	
2, 15	GND	These pins and exposed ground paddle must be connected to RF/DC ground.	
3	RFIN	This pin is DC coupled and matched to 50 Ohms.	
8, 23	Vgg2, Vgg1	Gate control for PA. Adjust Vgg to achieve recommended bias current. External bypass capacitors of 100 pF, 10 nF, and 4.7 µF are required. Apply Vgg bias to either pin 8 or pin 23.	
10, 11, 20, 21	Vdd3, Vdd4, Vdd2, Vdd1	Drain bias voltage for the amplifier. External bypass capacitors of 100 pF, 10 nF, and 4.7 µF are required.	
16	RFOUT	This pin is DC coupled and matched to 50 Ohms.	

Application Circuit



Evaluation PCB



List of Materials for Evaluation PCB EV1HMC7357LP5 [1]

Item	Description
J1 - J4	"K" Connector, SRI
J7, J8	DC Pin
C2, C3, C9, C12, C16, C19	100 pF Capacitor, 0402 Pkg.
C1, C4, C10, C11, C15, C20	10000 pF Capacitor, 0402 Pkg.
C21, C22, C25, C27, C28, C30	4.7 uF Capacitor, Case A Pkg.
R1, R2	43.2 Ohm Resistor, 0402 Pkg
U1	HMC7357LP5GE Amplifier
PCB [2]	600-00901-00 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Notes: