

Features

- Supply Voltage: 5 V
- Low Power Consumption: 15 mA/5 V
- Output Level and Spurious Products Adjustable (Optional)
- Excellent Sideband Suppression by Means of Duty Cycle Regeneration of the LO Input Signal
- Phase-control Loop for Precise 90° Phase Shifting
- Power-down Mode
- Low LO Input Level: -15 dBm
- 50-Ω Single-ended LO and RF Port
- LO Frequency Range of 30 MHz to 300 MHz

Benefits

- Low Current Consumption
- Few External Components Result in Cost and Board Space Saving
- Adjustment Free Hence Saves Time



300-MHz Quadrature Modulator

U2793B

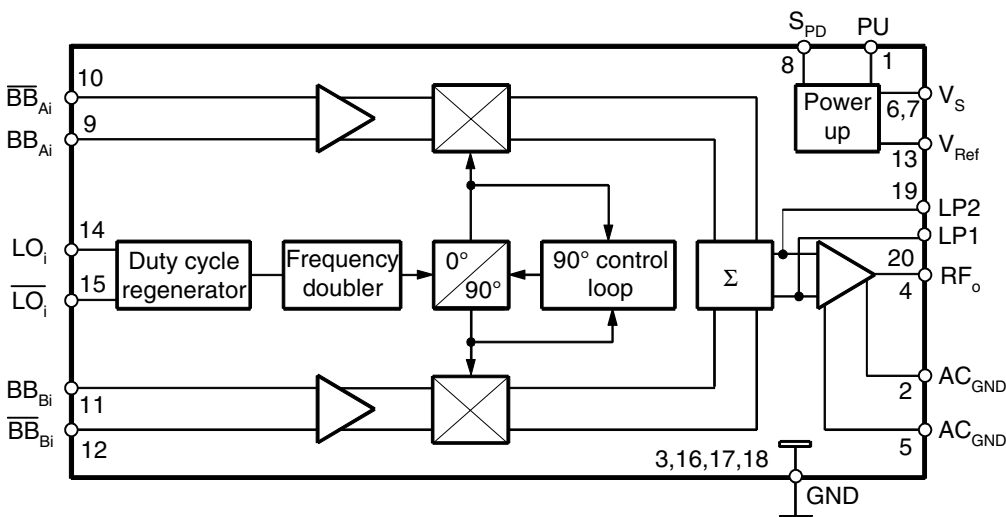
Electrostatic sensitive device.
Observe precautions for handling.



Description

The IC U2793B is a 300-MHz quadrature modulator that uses Atmel's advanced UHF process. It features low current consumption, single-ended RF ports and adjustment-free application, which makes the device suitable for all digital radio systems, e.g., GSM, PCN, JDC and WLAN. As an option, output level and spurious products are adjustable at pins 19 and 20. In conjunction with Atmel's U2795B mixer, an up-converter up to 2 GHz can be realized.

Figure 1. Block Diagram

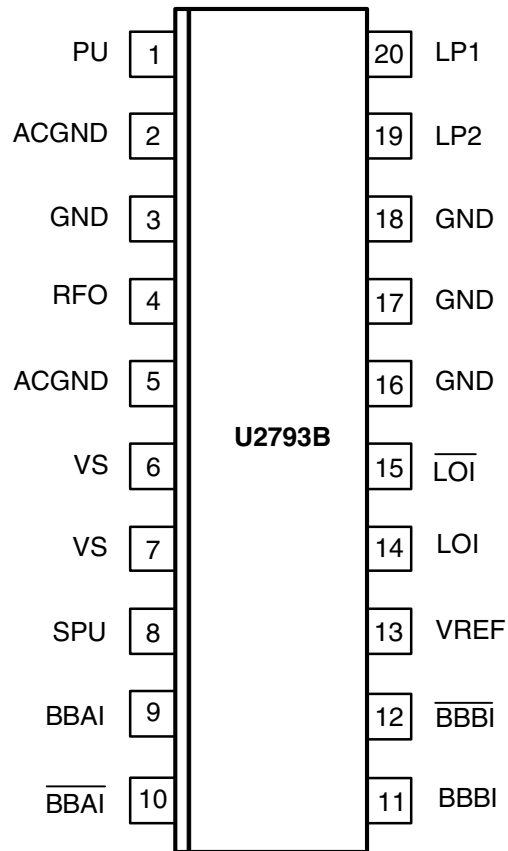


Rev. 4651B-CELL-06/04



Pin Configuration

Figure 2. Pinning SSO20



Pin Description

| Pin | Symbol | Function |
|-----|--------------------------|--------------------------------------|
| 1 | PU | Power-up input |
| 2 | ACGND | AC ground |
| 3 | GND | Ground |
| 4 | RFO | RF output |
| 5 | ACGND | AC ground |
| 6 | VS | Supply voltage |
| 7 | VS | Supply voltage |
| 8 | SPU | Settling time power-up |
| 9 | BBAI | Baseband input A |
| 10 | $\overline{\text{BBAI}}$ | Baseband input A inverse |
| 11 | BBBI | Baseband input B |
| 12 | $\overline{\text{BBBI}}$ | Baseband input B inverse |
| 13 | VREF | Reference voltage (2.5 V) |
| 14 | LOI | Input LO |
| 15 | $\overline{\text{LOI}}$ | Input LO inverse, typically grounded |
| 16 | GND | Ground |
| 17 | GND | Ground |
| 18 | GND | Ground |
| 19 | LP2 | Output low pass and power control |
| 20 | LP1 | Output low pass and power control |

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Value | Unit |
|---------------------------|-----------|-------------|------|
| Supply voltage | V_S | 6 | V |
| Input voltage | V_i | 0 to V_S | V |
| Junction temperature | T_j | 125 | °C |
| Storage temperature range | T_{Stg} | -40 to +125 | °C |

Thermal Resistance

| Parameters | Symbol | Value | Unit |
|------------------------|------------|-------|------|
| Junction ambient SSO20 | R_{thJA} | 140 | K/W |

Operating Range

| Parameters | Symbol | Value | Unit |
|---------------------------|-----------|------------|------|
| Supply voltage | V_S | 4.5 to 5.5 | V |
| Ambient temperature range | T_{amb} | -40 to +85 | °C |

Electrical Characteristics

Test conditions (unless otherwise specified); $V_S = 5\text{ V}$, $T_{amb} = 25^\circ\text{C}$, referred to test circuit.

System impedance $Z_o = 50\ \Omega$, $f_{LO} = 150\text{ MHz}$, $P_{LO} = -15\text{ dBm}$, $V_{BBI} = 1.0\text{ V}_{pp}$, differential

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|---|-----------------|------|-------------|------|----------------|------|------------|-------|
| 1.1 | Supply voltage range | | 6, 7 | V_S | 4.5 | 5 | 5.5 | V | A |
| 1.2 | Supply current | | 6, 7 | I_S | | 15 | | mA | A |
| 2 | Baseband Inputs, Pin 9-10, 11-12 | | | | | | | | |
| 2.1 | Input-voltage range (differential) | | | V_{BBI} | | 1000 | 1500 | mVpp | D |
| 2.2 | Input impedance | | | Z_{BBI} | | 30 | | k Ω | D |
| 2.3 | Input-frequency range | | | f_{BBI} | 0 | | 50 | MHz | D |
| 3 | LO Input, Pins 14 and 15 | | | | | | | | |
| 3.1 | Frequency range | | | f_{LOi} | 30 | | 300 | MHz | D |
| 3.2 | Input level ⁽¹⁾ | | | P_{LOi} | | -15 | -5 | dBm | D |
| 3.3 | Input impedance | | | Z_{iLO} | | ⁽²⁾ | | Ω | D |
| 3.4 | Voltage standing wave ratio | | | $VSWR_{LO}$ | | 3.5 | | | D |
| 3.5 | Duty-cycle range | | | DCR_{LO} | 0.4 | | 0.6 | | D |

- Notes:
1. Required LO level is a function of the LO frequency.
 2. The LO input impedance is consisting of a 50 Ω resistor in series with a 15 pF capacitor.
 3. With the pins 19 and 20 spurious performance especially for low frequency application can be improved by adding a chip capacitor between LP1 and LP2. In conjunction with a parallel resistor the output level can be adjusted to the following mixer stage without degradation of LO suppression and noise performance which would decrease if the I/Q input level is reduced
 4. For $T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$ and $V_S = 4.5\text{ V}$ to 5.5 V

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified); $V_S = 5\text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$, referred to test circuit.

System impedance $Z_o = 50\ \Omega$, $f_{\text{LO}} = 150\text{ MHz}$, $P_{\text{LO}} = -15\text{ dBm}$, $V_{\text{BBi}} = 1.0\text{ V}_{\text{pp}}$, differential (Continued)

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|-------------------------------------|---|-----|---------------------------|-------|--------------|-------|---------------|-------|
| 4 | RF Output, Pin 4 | | | | | | | | |
| 4.1 | Output level | $f_{\text{LO}} = 150\text{ MHz}$, $V_{\text{BBi}} = 1\text{ V}_{\text{pp}}$, differential $f_{\text{LO}} = 50\text{ MHz}$, $V_{\text{BBi}} = 0.3\text{ V}_{\text{pp}}$, differential | | P_{RFo} | -3 | -1 0 | +2 | dBm | A/B |
| 4.2 | LO suppression | $P_{\text{LO}} = -20\text{ dBm}$ | | LO_{RFo} | 32 | 45 | | dB | A |
| 4.3 | Voltage standing wave ratio | | | VSWR_{RF} | | 1.4 | 2 | | D |
| 4.4 | Sideband suppression ⁽³⁾ | | | SBS_{RFo} | 35 | 45 | | dB | A |
| 4.5 | Phase error ⁽⁴⁾ | | | P_e | | < 1 | | deg | D |
| 4.6 | Amplitude error | | | A_e | | < ± 0.25 | | dB | D |
| 4.7 | Noise floor | $V_{\text{BBi}} = 2\text{ V}$, $V_{\text{BBi}} = 3\text{ V}$ $V_{\text{BBi}} = V_{\text{BBi}} = 2.5\text{ V}$ | | N_{FL} | | -137 -143 | | dBm/Hz | D |
| 5 | Power-up Mode | | | | | | | | |
| 5.1 | Supply current | $V_{\text{PU}} \leq 0.5\text{ V}$, pins 6, 7 $V_{\text{PU}} = 1\text{ V}$ | | I_{PU} | | 10 | 1 | μA | D |
| 5.2 | Settling time | Pins 1 to 4, $C_{\text{SPU}} = 100\text{ pF}$ $C_{\text{LO}} = 100\text{ pF}$, $C_{\text{RFo}} = 1\text{ nF}$ | | t_{SPU} | | 10 | | μs | D |
| 6 | Switching Voltage, Pin 1 | | | | | | | | |
| 6.1 | Power on | | | V_{PUON} | 4 | | | V | D |
| 7 | Reference Voltage, Pin 13 | | | | | | | | |
| 7.1 | Voltage range | | | V_{Ref} | 2.375 | 2.5 | 2.625 | V | A |
| 7.2 | Output impedance | | | Z_{ORef} | | 30 | | Ω | D |

- Notes:
1. Required LO level is a function of the LO frequency.
 2. The LO input impedance is consisting of a $50\ \Omega$ resistor in series with a 15 pF capacitor.
 3. With the pins 19 and 20 spurious performance especially for low frequency application can be improved by adding a chip capacitor between LP1 and LP2. In conjunction with a parallel resistor the output level can be adjusted to the following mixer stage without degradation of LO suppression and noise performance which would decrease if the I/Q input level is reduced
 4. For $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$ and $V_S = 4.5\text{ V}$ to 5.5 V

Figure 3. Reference Voltage versus T_{amb}

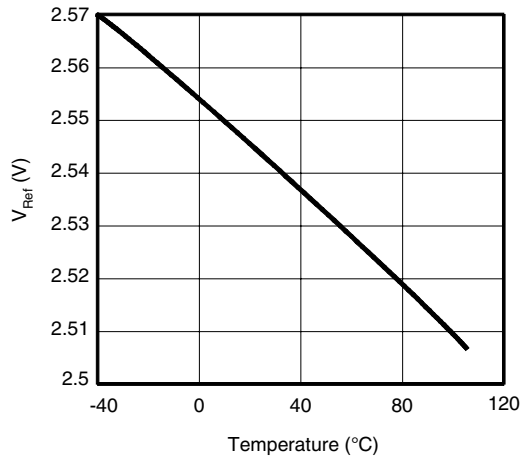


Figure 4. OIP3 versus T_{amb} , LO = 150 MHz, Level -10 dBm

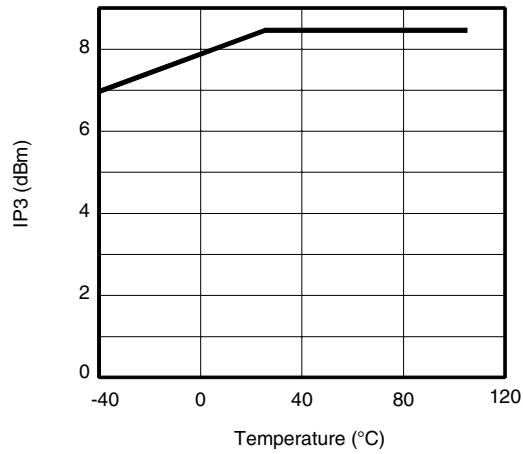


Figure 5. Supply Current versus T_{amb}

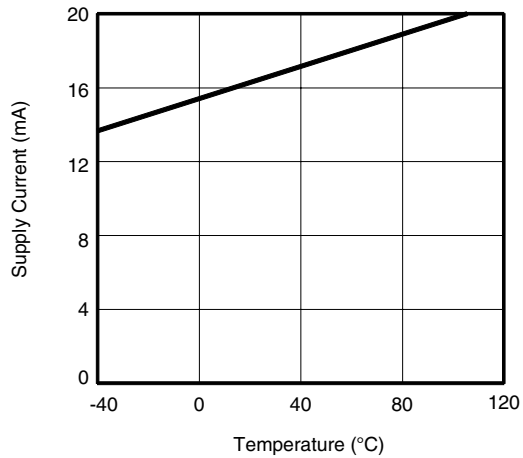


Figure 6. Recommended LO Power Range versus LO Frequency at $T_{amb} = 25^{\circ}C$

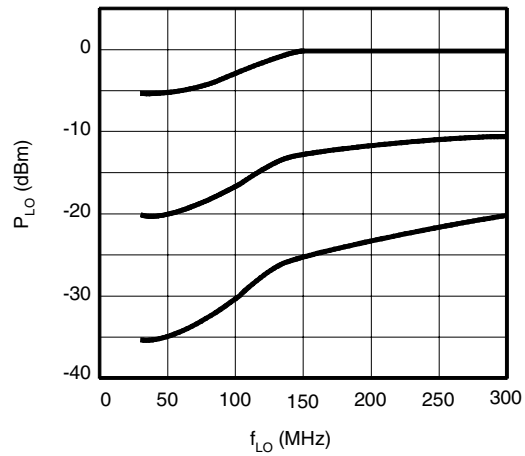


Figure 7. Output Power versus T_{amb}

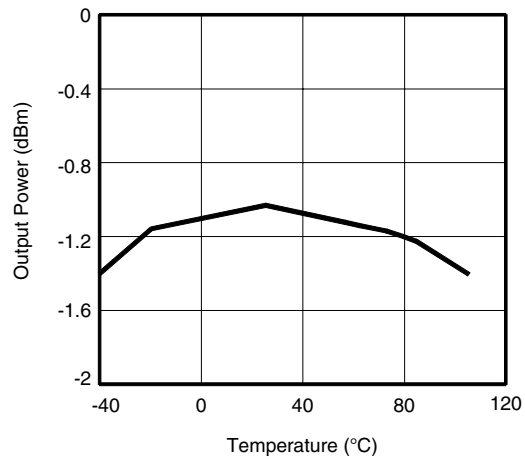


Figure 8. Typical Output Power versus LO Frequency at $T_{amb} = 25^{\circ}C$, $V_{BBI} = 250$ mV (differential)

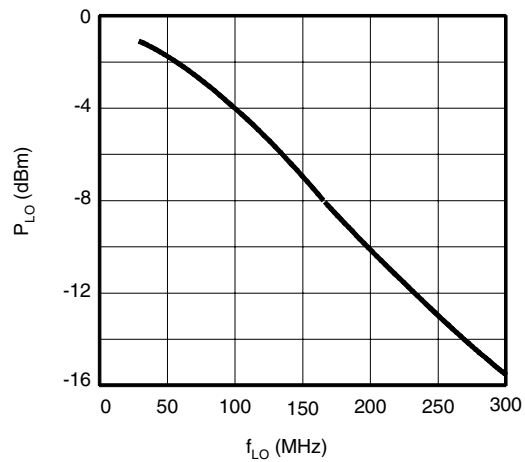


Figure 9. Typical Required V_{BBi} Input Signal (Differential) versus LO Frequency for $P_{\text{O}} = 1 \text{ dBm}$ and $P_{\text{O}} = -3 \text{ dBm}$

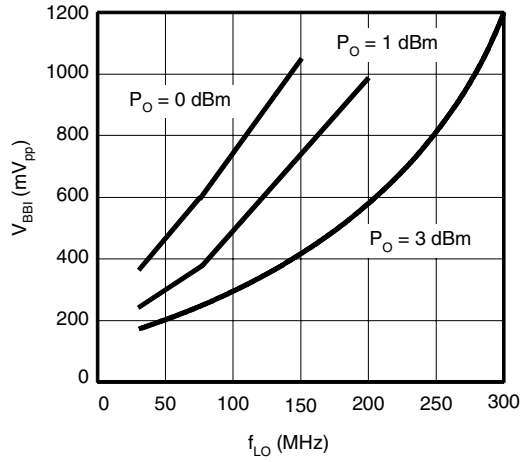
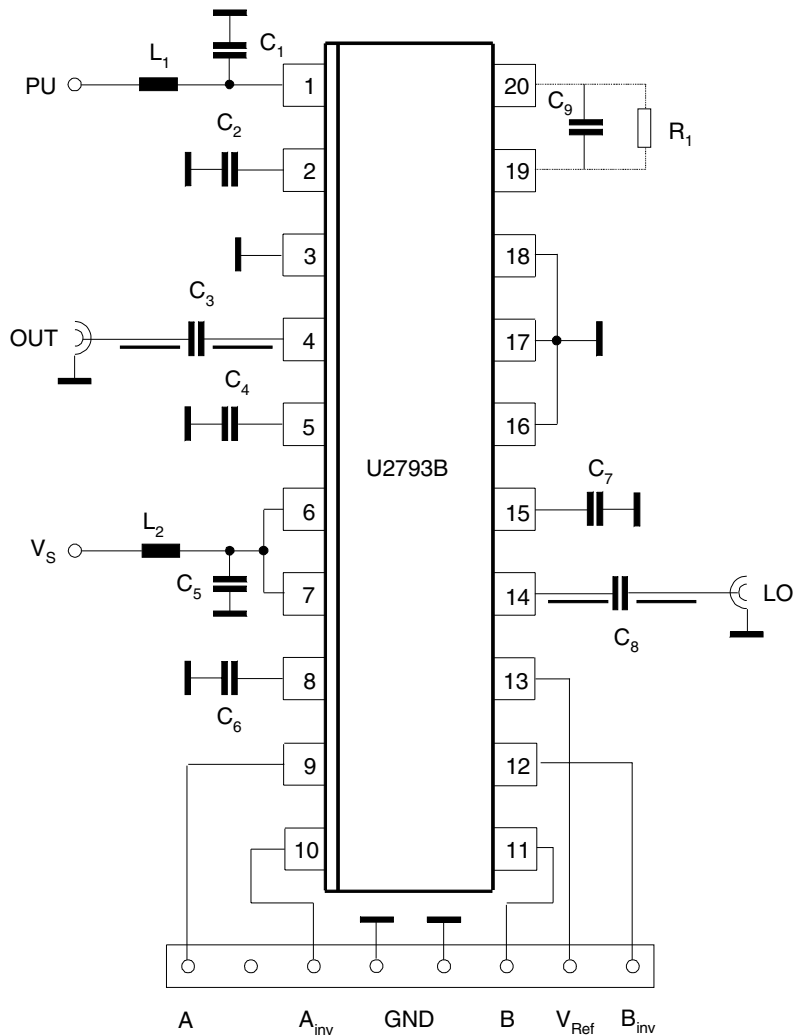


Figure 10. Evaluation Board Circuitry

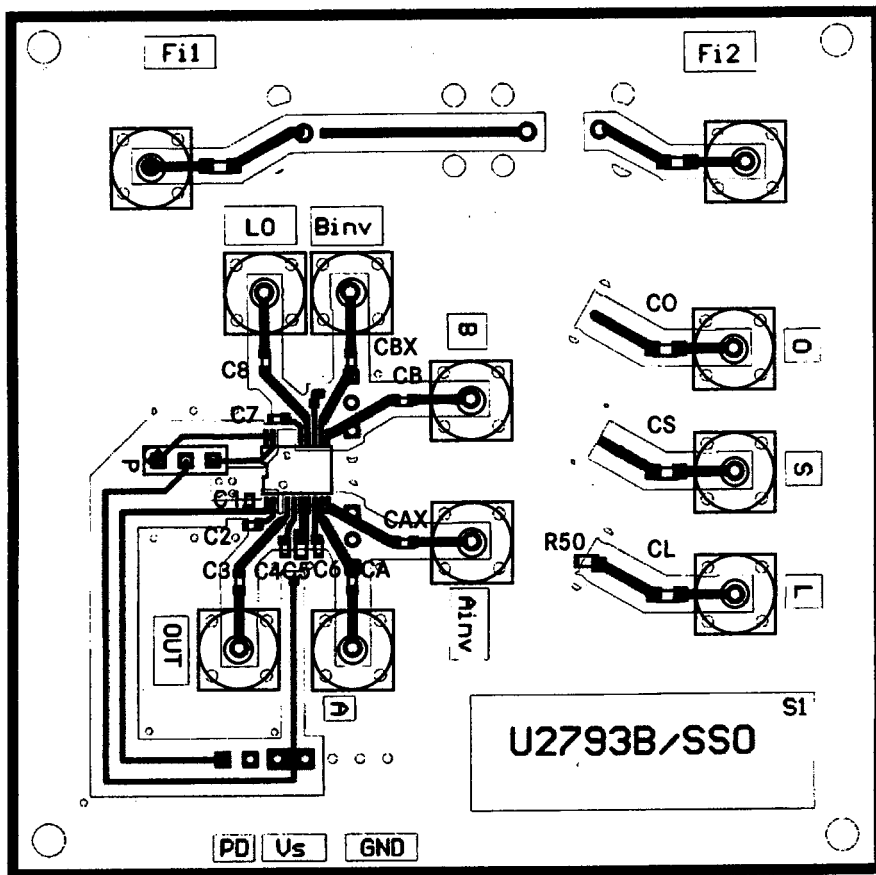


Part List

| | |
|---------------------------|-----------------|
| C_1, C_2, C_3, C_4, C_6 | 1 nF |
| C_7, C_8 | 100 pF |
| C_5 | 100 nF |
| C_9, R_1 | 1 pF to 10 pF |
| ===== | 50-Ω Microstrip |
| ----- | optional |

The above listed components result in a PD settling time of < 20 μs. The use of other component values will require consideration for time requirements in burst-mode applications.

Figure 11. PCB Layout Evaluation Board



Application Circuits

Bias network for AC-coupled baseband inputs (V_{BA} , V_{BB}).

$R_1 = 2.5 \text{ k}\Omega$, $R_2 \leq 10 \text{ k}\Omega$ for $\geq 35 \text{ dB}$ LO suppression which is in reference to $< 2 \text{ mV}$ input offset.

Figure 12. Application Circuit with AC-coupled Baseband Inputs

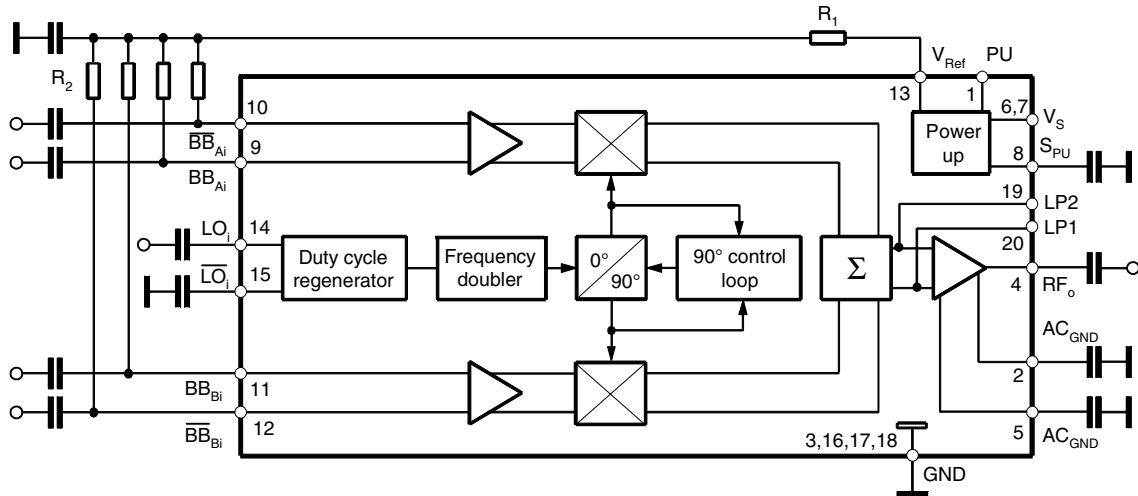
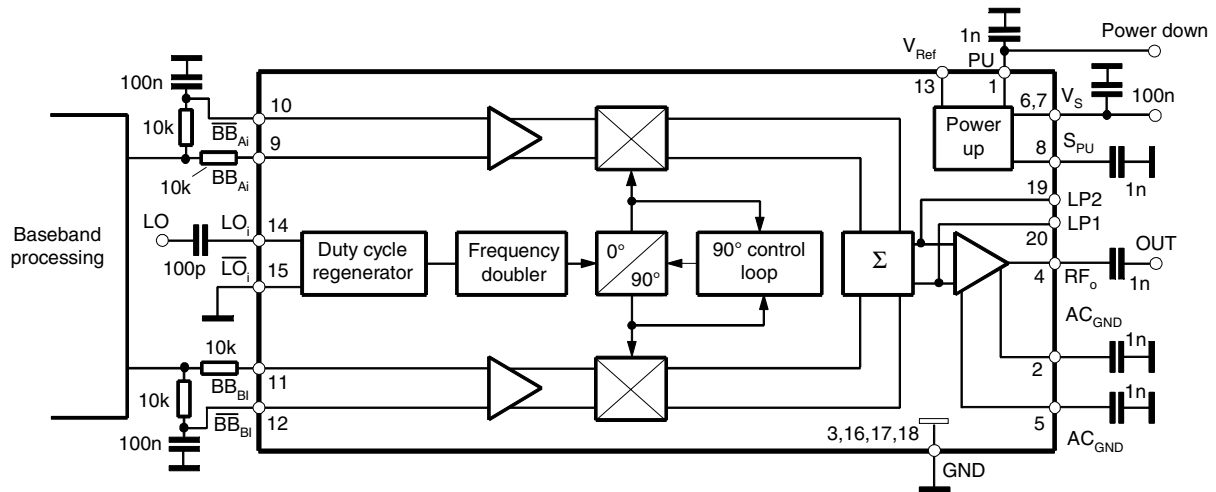


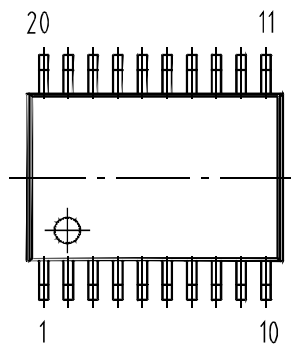
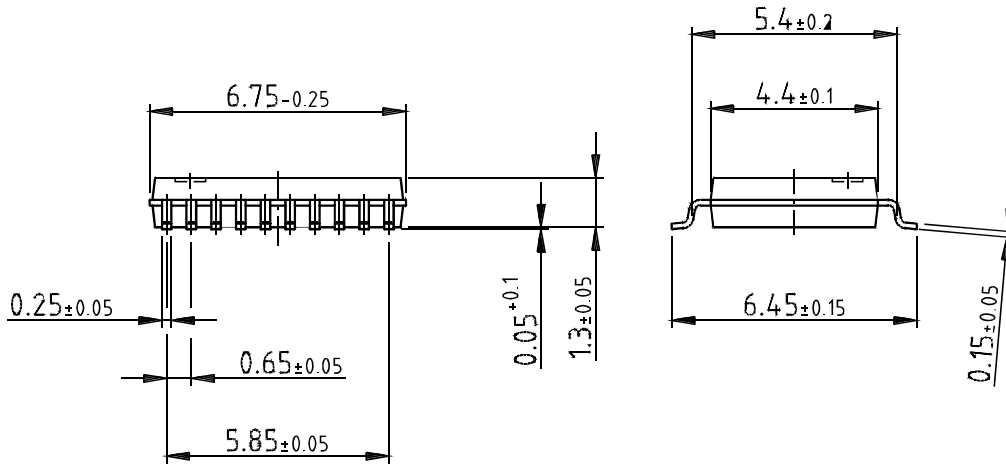
Figure 13. Application Circuit with DC-coupled Baseband Inputs



Ordering Information

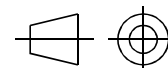
| Extended Type Number | Package | Remarks |
|----------------------|---------|-----------------------------|
| U2793B-MFS | SSO20 | Tube |
| U2793B-MFSG3 | SSO20 | Taped and reeled |
| U2793B-MFSH | SSO20 | Tube, lead free |
| U2793B-MFSG3H | SSO20 | Taped and reeled, lead free |

Package Information



Package: SSO 20

Dimensions in mm



Technical drawings according to DIN specifications

Drawing-No.: 6.543-5056.01-4

Issue: 1; 10.03.04



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenalux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

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San Jose, CA 95131, USA
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Maxwell Building
East Kilbride G75 0QR, Scotland
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Fax: (44) 1355-242-743

RF/Automotive

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Fax: (49) 71-31-67-2340

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