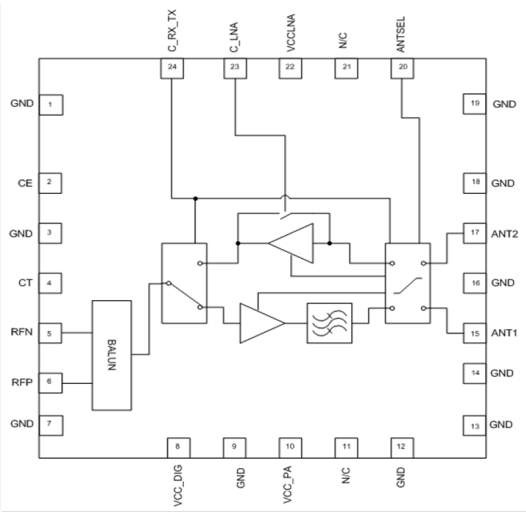
RFMD + TriQuint = Qorvo

RF6555

2.0V TO 3.6V, 2.4GHz FRONT END MODULE

The RF6555 integrates a complete solution in a single Front End Module (FEM) for WiFi and ZigBee® applications in the 2.4GHz to 2.5GHz band. This FEM integrates the PA plus harmonic filter in the transmit path. The RF6555 also has an integrated LNA with bypass mode internally. The RF6555 provides a single balanced TDD access for Rx and Tx paths along with two ports on the output for connecting a diversity solution or a test port. The device is provided in a 5mm x 5mm x 1mm, 24-pin laminate package.



Functional Block Diagram

Package: Laminate, 24-Pin, 5mm x 5mm x 1mm

Features

- Tx Output Power = 18dBm
- Integrated RF Front End Module with Rx Balun, PA, Filter, LNA with Bypass Mode, and DP2T Switch
- Single Bidirectional Differential Transceiver Interface.
- Voltage Range = 2.0V to 3.6V

Applications

- ZigBee® 802.15.4 Based Systems for Remote Monitoring and Control
- Set-top Boxes
- AA Battery Operation
- 2.4GHz ISM Band Applications
- Smart Meters for Energy Management

Ordering Information

RF6555SB	Standard 5-piece sample bag
RF6555SQ	Standard 25-piece sample bag
RF6555SR	Standard 100-piece reel
RF6555TR13	Standard 2500-piece reel
RF6555PCK-410	Fully assembled eval board w/ 5-piece sample bag

Absolute Maximum Ratings

Parameter	Rating	Unit
DC Supply Voltage	5.0	V
DC Supply Current	150	mA
Operating Case Temperature	-40 to +85	ºC
Storage Temperature	-40 to +150	ºC
ESD Human Body Model RF Pins	1000	V
ESD Human Body Model All Other Pins	500	V
ESD Charge Device Model All Pins	500	V
Moisture Sensitivity Level	MSL 2	
Maximum Tx Input Power	+5	dBm
Maximum Rx Input Power	+8	dBm

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

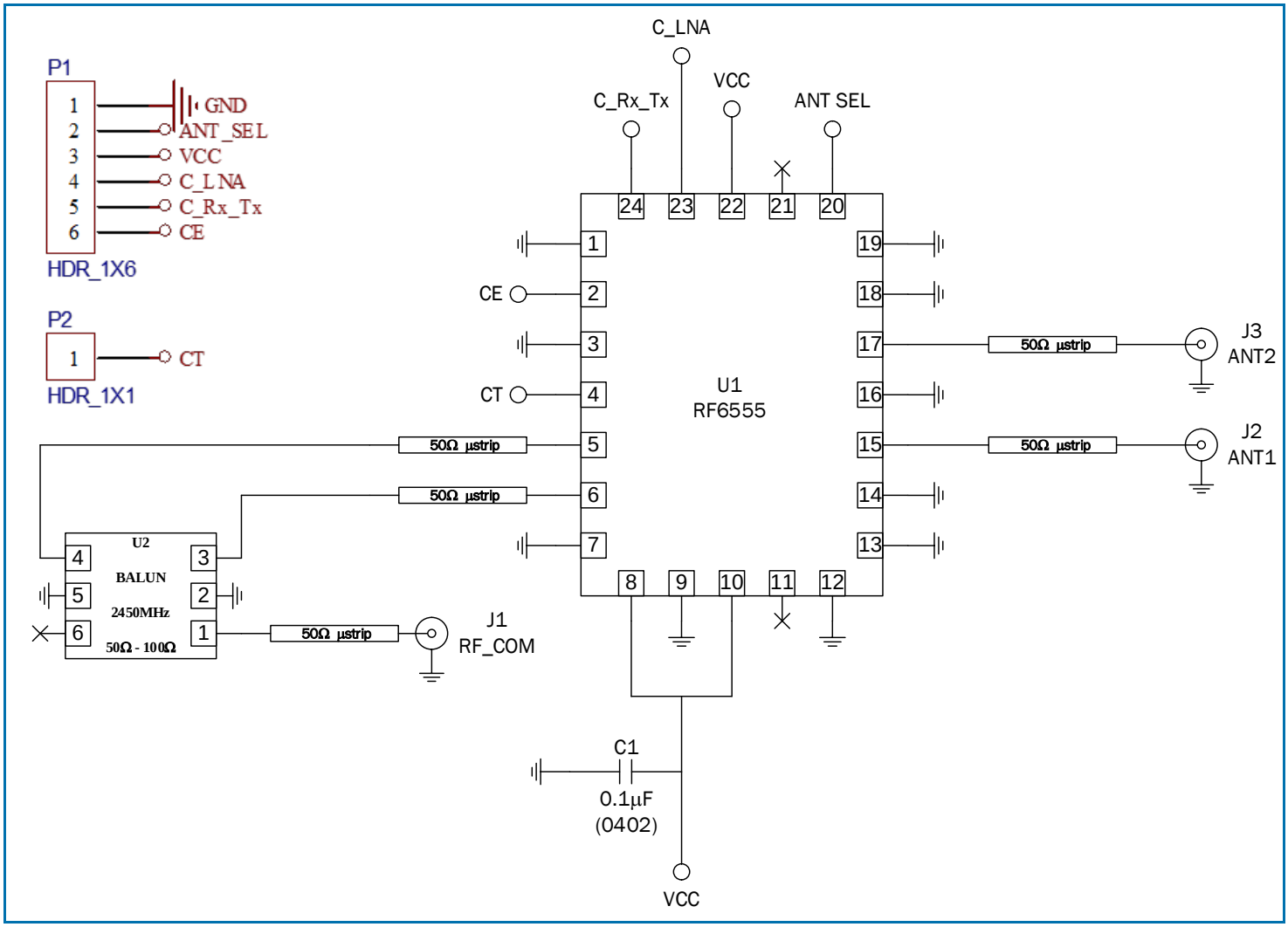
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Parameter					
V_{BATT}	2.0	3.0	3.6	V_{DC}	
Operating Temperature Range	-40	+25	+85	ºC	
Z_O		50		Ω	
Off Mode Current		0.05	1.0	µA	All logic low, Temp = 25°C; Over Voltage.
Storage Temperature	-40		+150	°C	
ESD, HBM	1000			V	RF pins
ESD, HBM	500			V	All other pins
ESD, CDM	500			V	All pins
MSL	MSL3				
Current Sourced through CT Pin			18	mA	
Voltage Drop from CT Pin to RXP/RXN			0.1	V	
Tx Path					
Frequency	2405		2480	MHz	
Input Return Loss	10			dB	Pins 5, 6 (RFM, RFP) 100Ω differential
Output Return Loss	10			dB	
Gain	22	25		dB	2.7V to 3.6V
	21			dB	V_{CC}=2.0V; Temp=25°C
Gain Flatness	-0.8		+0.8	dB	
Rated Output Power	20			dBm	Nominal conditions (V_B=3.3 to 3.6, All Temp)
	18			dBm	Nominal conditions (V_B=3.0 to 3.3, All Temp)
	16			dBm	Nominal conditions (V_B=2.7, All Temp)
	14			dBm	Nominal conditions (V_B=2.0, All Temp)
Saturated Output Power		22		dBm	V_B=3.6, Temp = 25C
		20		dBm	V_B=3.0, Temp = 25C
Supply Current		110	125	mA	P_O =21dBm 802.15.4 OQPSK (V_B=3.6, All Temp)
		105	120	mA	P_O =20dBm 802.15.4 OQPSK (V_B=3.0, All Temp)
		70	95	mA	P_O =18dBm 802.15.4 OQPSK (V_B=3.0, All Temp)

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
		50		mA	P_O =14dBm 802.15.4 OQPSK (V_B=2.0, All Temp)
Thermal Resistance		78		°C/W	V_{CC} = 3.0V, P_{OUT} = 18dBm, T_{REF} = 85°C
Harmonics 2f0 to 5f0		-45	-42	dBm/MHz	At 18dBm, V_{CC} = 3.0V to 3.6V
VSWR Stability and Load	4:1				
VSWR No Damage	8:1				
Gain Settling Time		1	10	µS	
Rx Path					
Frequency	2405		2480	MHz	
Gain	8.5	11	13	dB	
Noise Figure		3		dB	Temp = 25°C; over voltage and frequency
Current		8	12	mA	Nominal conditions
IIP3		7		dBm	
Gain Flatness	-0.5		+0.5	dB	
Input Return Loss	10	15		dB	
Output Return Loss	10			dB	Pins 5, 6 (RFM, RFP) 100Ω differential
Amplitude Imbalance	-1		+1	dB	
Phase Imbalance	-15		+15	dB	
Maximum Input Power	5			dBm	
Bypass Mode					
Frequency	2405		2480	MHz	
Insertion Loss/Noise Figure		5	6.5	dB	SW1dB, Bypass 2.5dB, Balun 1.5dB
Current		50		µA	
IIP3		23		dBm	
Gain Flatness	-0.5		0.5	dB	
Input Return Loss	10	12		dB	
Output Return Loss	10			dB	Pins 5, 6 (RFM, RFP) 100Ω differential
Amplitude Imbalance	-1		+1	dB	
Phase Imbalance	-15		+15	dB	
Maximum Input Power	10			dBm	
Logic					
Logic Level “HIGH” Input Voltage	V_{BATT} -0.2		V_{BATT}	V	
Logic Level “LOW” Input Voltage	0.0		0.2	V	
Input Source Current at Logic “HIGH”		5	10	µA	
Switch Leakage Current at Logic “LOW”			1	µA	
Antenna Switch					
RF to Control Isolation		50		dB	
ANT1 to ANT2 Isolation		20		dB	
T/R Switching Time			1	µS	

Control Logic Table

Mode	CE	C_RX_TX	C_LNA	ANTSEL
TX-ANT1	High	High	Low	Low
TX-ANT2	High	High	Low	High
RX-ANT1 LNA	High	Low	Low	Low
RX-ANT1 BYP	High	Low	High	Low
RX-ANT2 LNA	High	Low	Low	High
RX-ANT2 BYP	High	Low	High	High
Power Down	Low	Low	Low	Low

Applications Schematic



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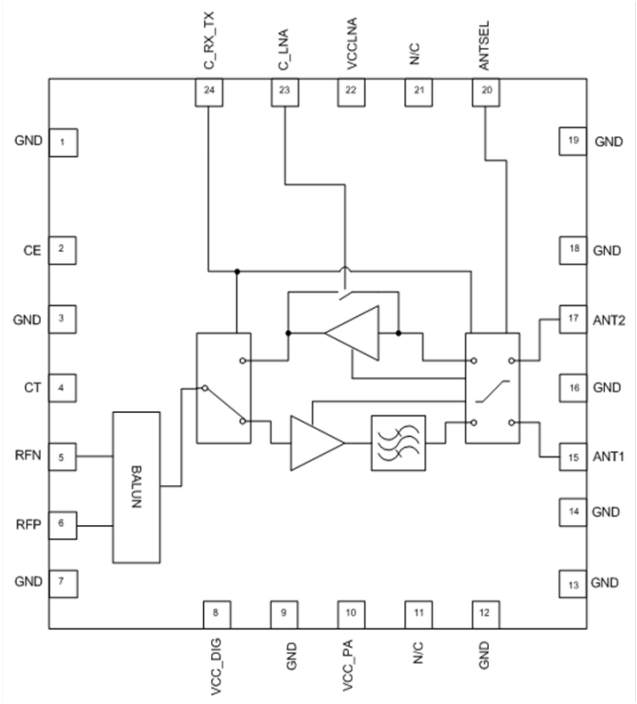
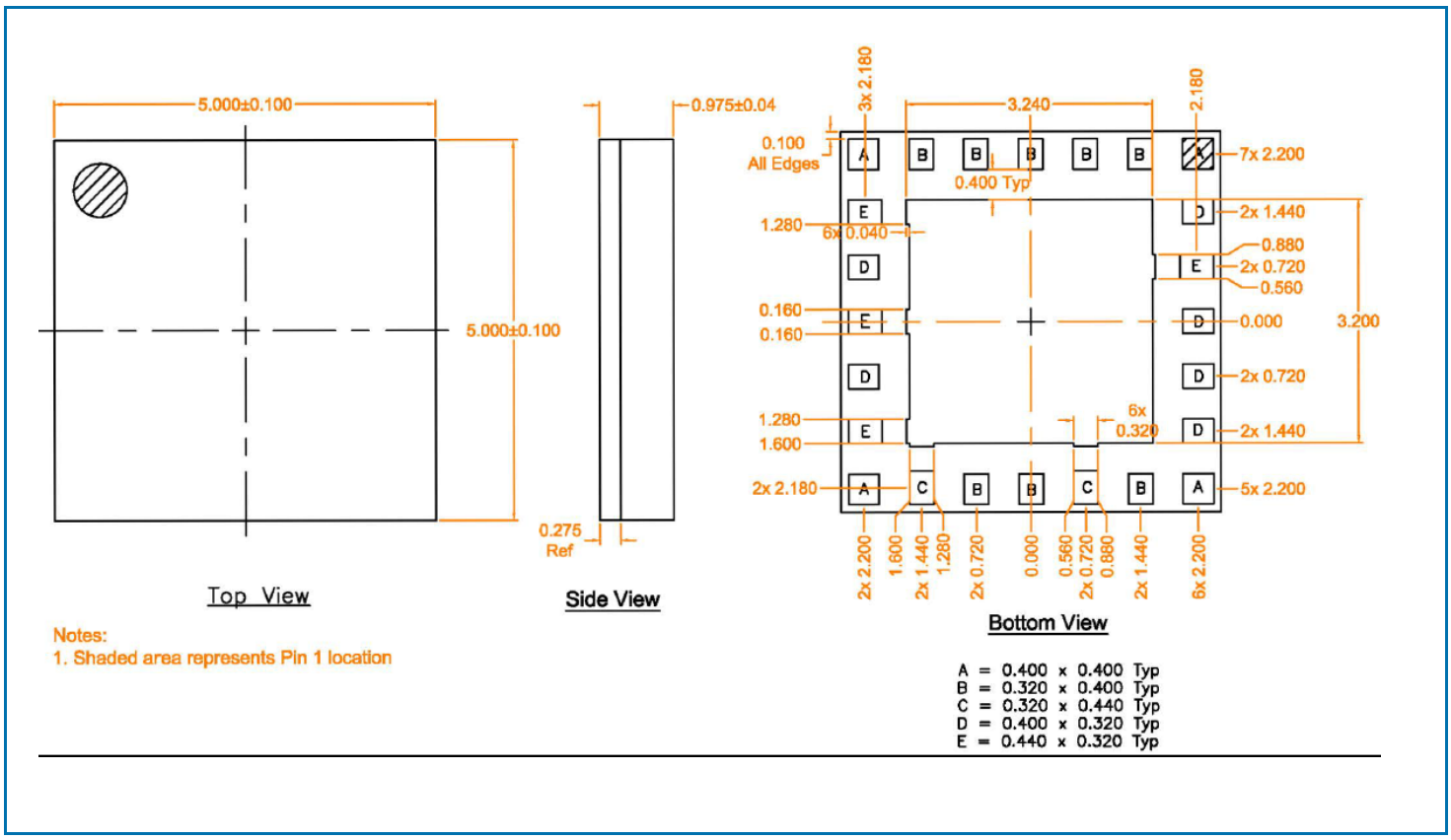
Pin Out

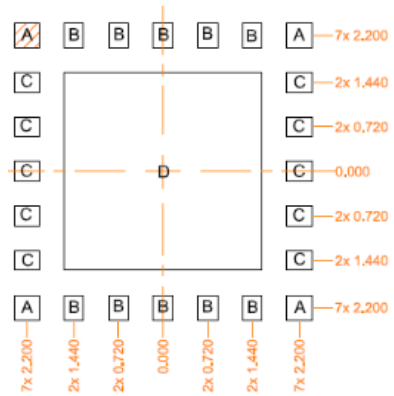


Package Drawing



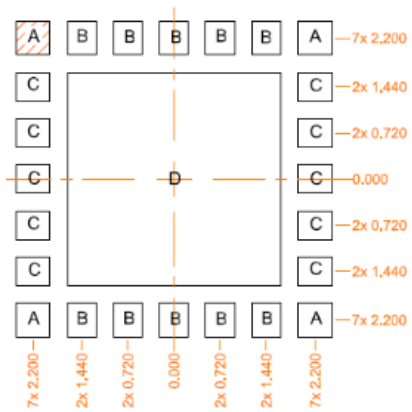
Notes:
1. Shaded area represents Pin 1 location

PCB Patterns



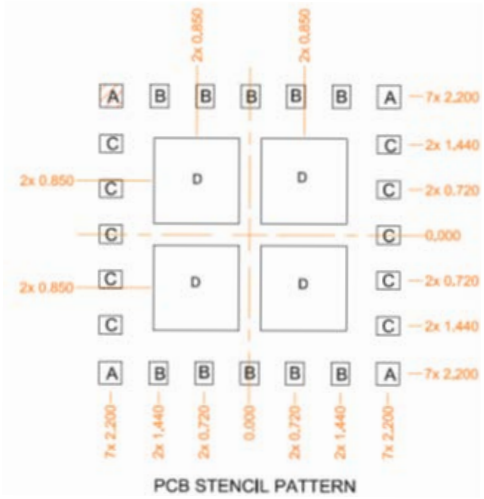
PCB METAL LAND PATTERN

A= 0.400 x 0.400 mm
B= 0.320 x 0.400 mm
C= 0.400 x 0.320 mm
D = 3.200 x 3.200 mm



PCB SOLDER MASK LAND PATTERN

A= 0.530 x 0.530 mm
B= 0.450 x 0.530 mm
C= 0.530 x 0.450 mm
D = 3.330 x 3.330 mm



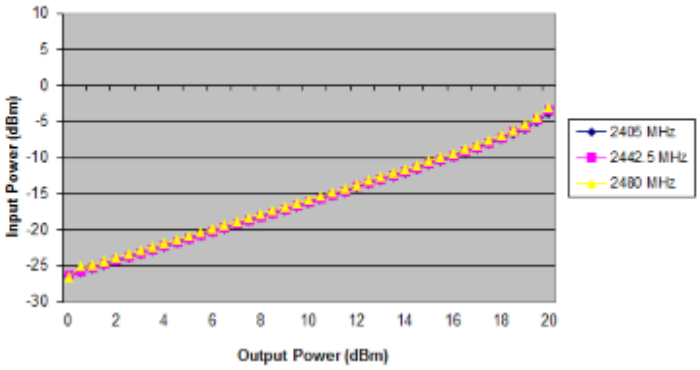
PCB STENCIL PATTERN

A= 0.360 x 0.360 mm
B= 0.288 x 0.360 mm
C= 0.360 x 0.288 mm
D = 1.350 x 1.350 mm

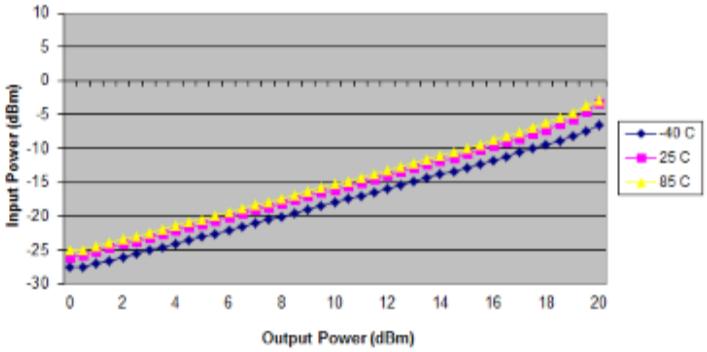
Thermal vias for center slug “D” should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, power dissipation and electrical requirements. Example of the number and size of vias can be found on the RFMD evaluation board layout (gerber files are available upon request).

RF6555 2.4 GHz Front End Module

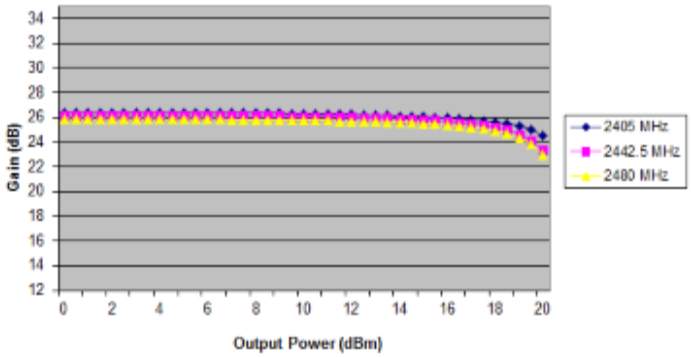
Input Power vs Output Power
Vcc = 3.0V; TX_EN = 3.0V



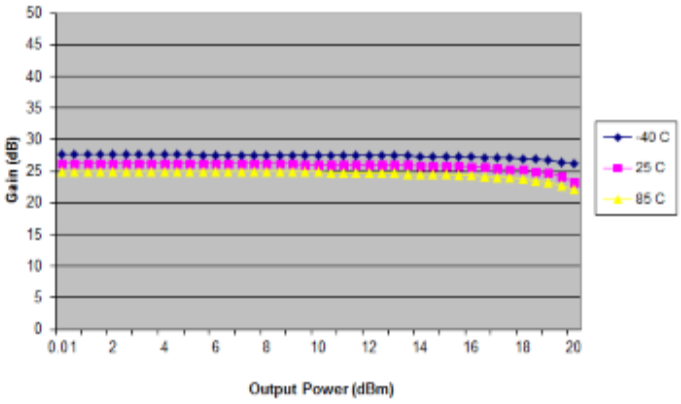
Input Power vs Output Power
(Over Temperature @ 2442.5 MHz)
Vcc = 3.0V; TX_EN = 3.0V



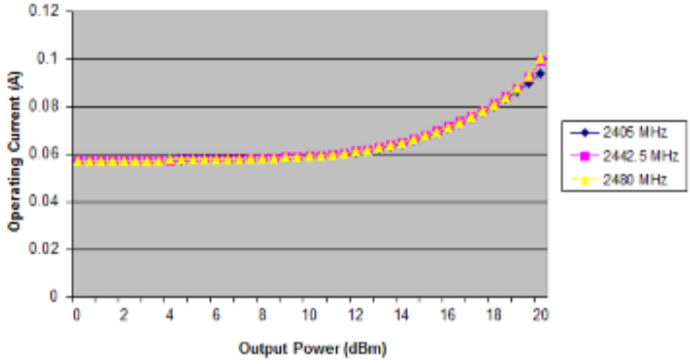
Gain vs Output Power
Vcc = 3.0V; TX_EN =3.0V



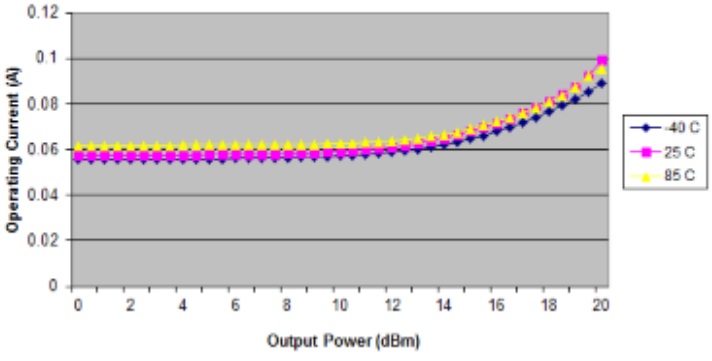
Gain vs Output Power
(Over Temperature @ 2442.5 MHz)
Vcc = 3.0V; TX_EN = 3.0V



Operating Current vs Output Power
Vcc = 3.0V; TX_EN = 3.0V



Operating Current vs Output Power
(Over Temperature @ 2442.5 MHz)
Vcc = 3.0V; TX_EN = 3.0V



Pin Names and Descriptions

Pin	Name	Description
1	GND	Ground.
2	CE	Control voltage pin for chip enable. See logic table.
3	GND	Ground.
4	CT	Center tap for passing DC voltage to RFN/RFP pins that connect to the TXVR SoIC.
5	RFN	Differential bi-directional RF port. Matched to 50Ω single-ended, 100Ω differential.
6	RFP	Differential bi-directional RF port. Matched to 50Ω single-ended, 100Ω differential.
7	GND	Ground.
8	VCC_DIG	Voltage supply pin for digital logic circuitry.
9	GND	Ground.
10	VCC_PA	Voltage supply pin for Tx power amplifier.
11	N/C	Not connected.
12	GND	Ground.
13	GND	Ground.
14	GND	Ground.
15	ANT1	Antenna port 1. Match to 50Ω and DC blocked internally.
16	GND	GND Ground.
17	ANT2	Antenna port 2. Matched to 50Ω and DC blocked internally.
18	GND	Ground.
19	GND	Ground.
20	ANTSEL	Control pin for antenna selection. See logic table.
21	N/C	Not connected.
22	VCC_LNA	Voltage supply pin for Rx low noise amplifier.
23	C_LNA	Control voltage for pin for LNA/bypass modes. See logic table.
24	C_RX_TX	Control voltage pin for Tx/Rx modes. See logic table.