XP1039-QJ

2.5W Power Amplifier
5.6 - 7.1 GHz

Preliminary - Rev. V1P
Mimix Broadband

Features

- 17 dB Small Signal Gain
- 48 dBm Third Order Intercept Point (OIP3)
- 2.5W Saturated RF Power
- Integrated Power Detector
- Lead-Free 6 mm 24-lead QFN Package
- RoHS* Compliant and 260°C Reflow Compatible

Description

The XP1039-QJ is a packaged linear power amplifier that operates from 5.6-7.1 GHz. The device provides 17 dB gain and 48 dBm Output Third Order Intercept Point (OIP3) with up to 2.5W of saturated RF power. The packaged amplifier comes in an industry standard, fully molded 6x6 mm QFN package and is comprised of a two stage power amplifier with an integrated, temperature compensated on-chip power detector. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly of the packaged part. The device is specifically designed for use in PtP radio applications and is well suited for other telecom applications such as SATCOM and VSAT.

Preliminary

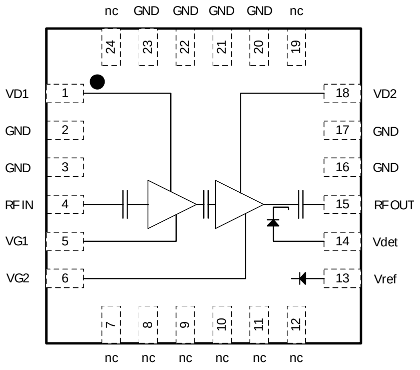
Pin Configuration

Pin No.	Function	Pin No.	Function
1	Drain 1 Bias	14	Power Detector
2-3	Ground	15	RF Output
4	RF Input	16-17	Ground
5	Gate 1 Bias	18	Drain 2 Bias
6	Gate 2 Bias	19	Not Connected
7-12	Not Connected	20-23	Ground
13	Power Det. Ref.	24	Not Connected

Ordering Information

Part Number	Package
XP1039-QJ-0G00	bulk quantity
XP1039-QJ-0G0T	tape and reel
XP1039-QJ-EV1	evaluation module

Functional Schematic



Absolute Maximum Ratings [1,2,3]

Parameter	Absolute Max.
Supply Voltage (Vd)	+8.0 V
Supply Voltage (Vg)	-2.5 V
Supply Current (Id1)	600 mA
Supply Current (Id2)	1200 mA
Detector Pin (Vdet)	6 V
Detector Ref Pin (Vref)	6 V
Input Power (Pin)	+23 dBm
Abs. Max Junction/Channel Temp.	175 ºC
Max. Operating Junction/Channel Temp.	160 ºC
Continuous Power Dissipation (Pdiss) at 85 ºC	11.2W
Thermal Resistance (Tchannel=160 ºC)	6.8 ºC/W
Operating Temperature (Ta)	-40 °C to +85 °C
Storage Temperature (Tstg)	-65 °C to +150 °C
Mounting Temperature	See solder reflow profile
ESD Min.-Machine Model (MM)	Class A
ESD Min.-Human Body Model (HBM)	Class 1A
MSL Level (MSL)	MSL3

1. Operation of this device above any one of these parameters may cause permanent damage.
2. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.
3. For saturated performance it recommended that the sum of (2*Vdd + abs(Vgg)) <17

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Electrical Specifications: Vdd = 7V, Idq[5] = 1350 mA, T_A[4] = +25°C

Parameter	Units	Min.	Typ.	Max.
Small Signal Gain (S21)	dB		17.0	
Input Return Loss (S11)	dB		10.0	
Output Return Loss (S22)	dB		8.0	
P1dB	dBm		33.0	
Psat	dBm		34.0	
Output IP3, +22 dBm SCL	dBm		48	
Detector Power Range	dBm	0.0	-	34.0
Detector Bias Voltage (Vdet,ref)	VDC		5.0	
Gate Bias Voltage (V_{GG}1,2)	VDC		-0.9	

4. T_A = Ambient Temperature
5. Adjust V_{GG1} and V_{GG2} between –1.4 and –0.4V to achieve specified I_{DQ}. V_{GG1} and V_{GG2} should be the same voltage.

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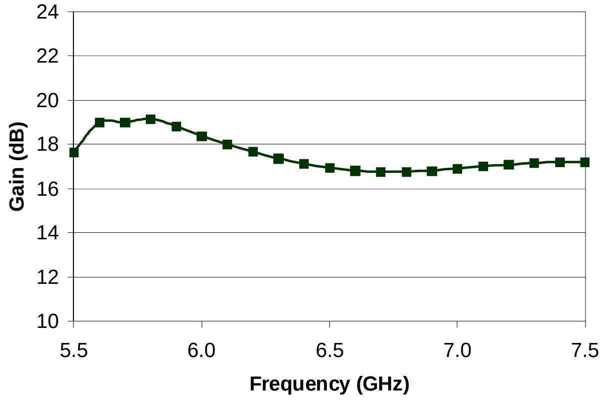
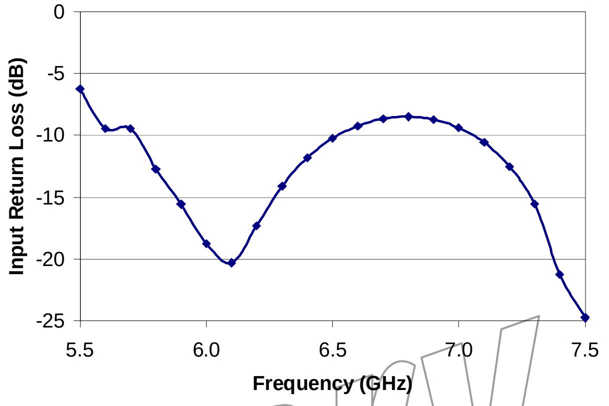
Typical Performance Curves: Vdd = 7V, Idq = 1350 mA

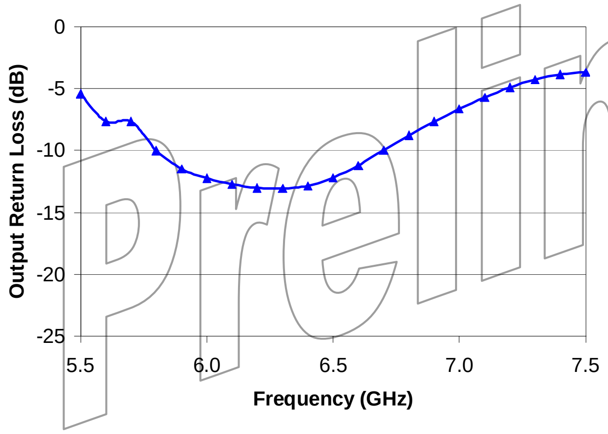
Gain vs. Frequency, 25C



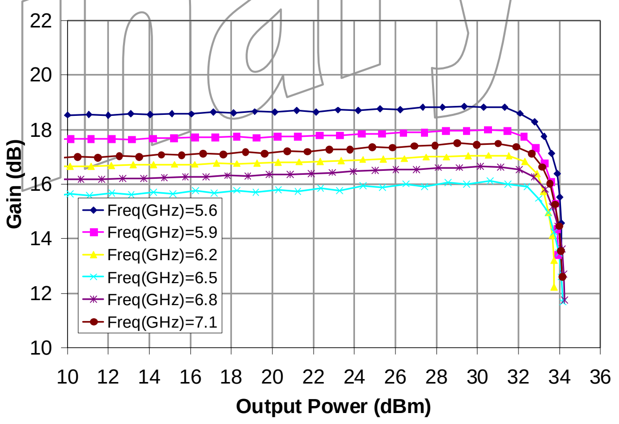
Input Return Loss vs. Frequency, 25C



Output Return Loss vs. Frequency, 25C



Gain vs. Output Power, 25C



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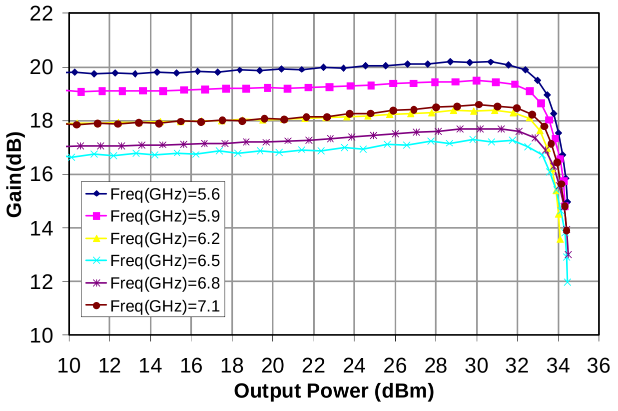
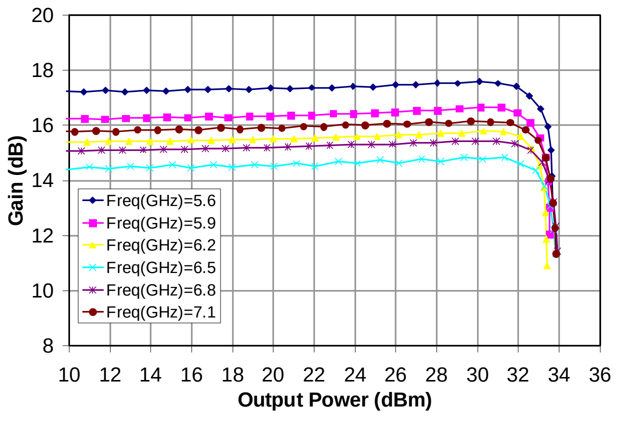
Gain vs. Output Power, -40C



Gain vs. Output Power, +85C



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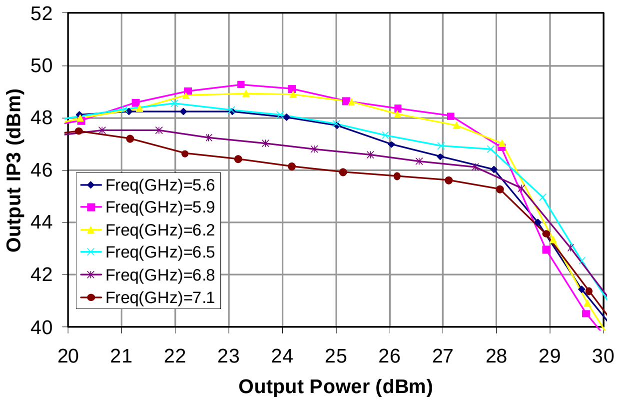
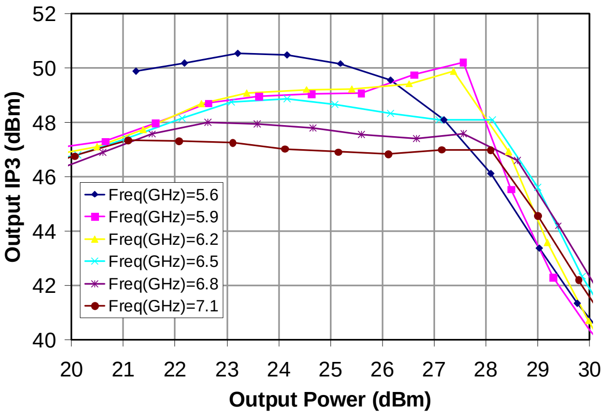
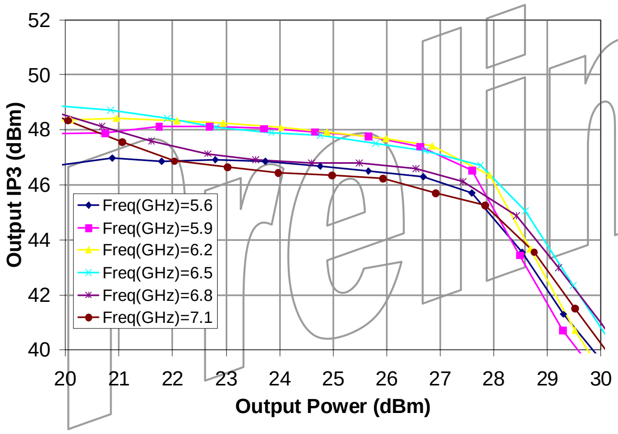
Output IP3 vs. Output Power, 25C



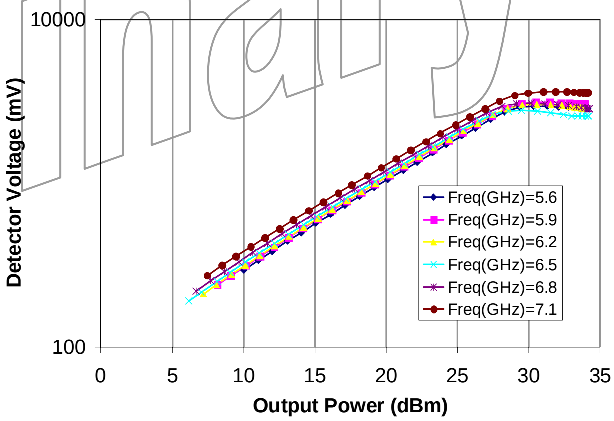
Output IP3 vs. Output Power, -40C



Output IP3 vs. Output Power, +85C



Detector Voltage vs. Output Power, 25C



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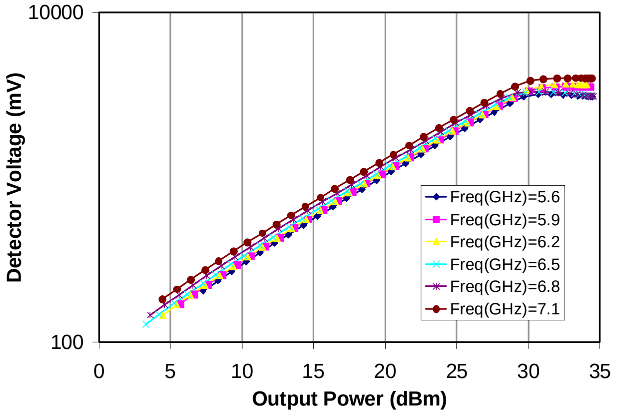
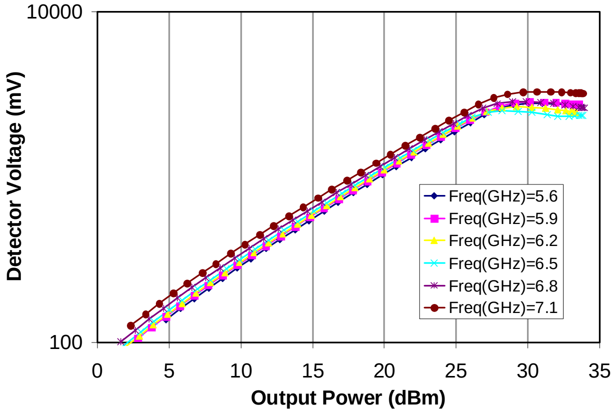
Detector Voltage vs. Output Power, -40C



Detector Voltage vs. Output Power, +85C



App Note [1] Biasing - As shown in the Pin Designations table, the device is operated by biasing Vd1,2 at 7.0V. The nominal drain currents are Id1=450mA and Id2=900mA. This ratio of 1:2 between the first and second stage drain currents should be maintained for best linearity. The typical gate voltages needed are -0.9V. The negative gate voltage must be applied prior to applying the positive drain voltage.

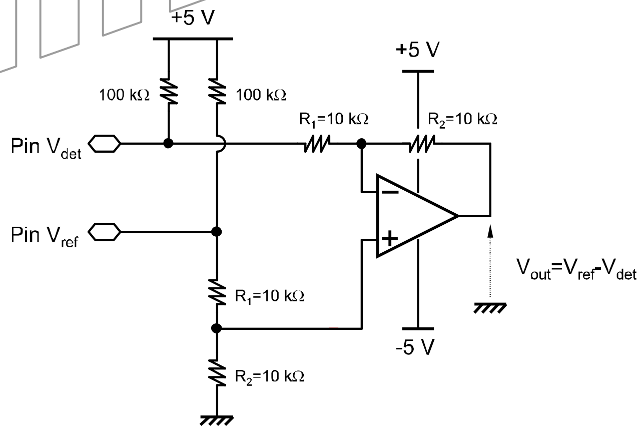
For linear applications it is recommended that active bias be used to keep the currents known and constant, and to maintain the best performance over temperature. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low-power operational amplifier, with a low value resistor in series with the drain supply used to sense the current.

For applications where the device is running into saturation, high power levels will be achieved by fixing the drain currents at the nominal levels with NO RF applied, and then operated with a fixed gate bias once RF is applied.

App Note [2] PWB Layout Considerations - It is recommended to provide 100pF decoupling capacitors as close as possible to the pins of the device, with additional larger decoupling capacitors further away. For example, in the Recommended Layout shown below, there are 100pF 0402 capacitors placed very near the device pins, and 1uF 0805 capacitors placed further away (the gate line shown without a 1uF capacitor (pin 6) would have this capacitor further away on the other side of the screw).

Thermal management of the device is essential. It is recommended that measures such as copper-filled vias under the package, and post/screws for top to bottom heat transfer are used (see Recommended Layout shown below). Adequate heat-sinking under the PWB is necessary in maintaining the package base at a safe operating temperature.

App Note [3] Power Detector - As shown in the schematic at right, the power detector is implemented by providing +5V bias and measuring the difference in output voltage with standard op-amp in a differential mode configuration.



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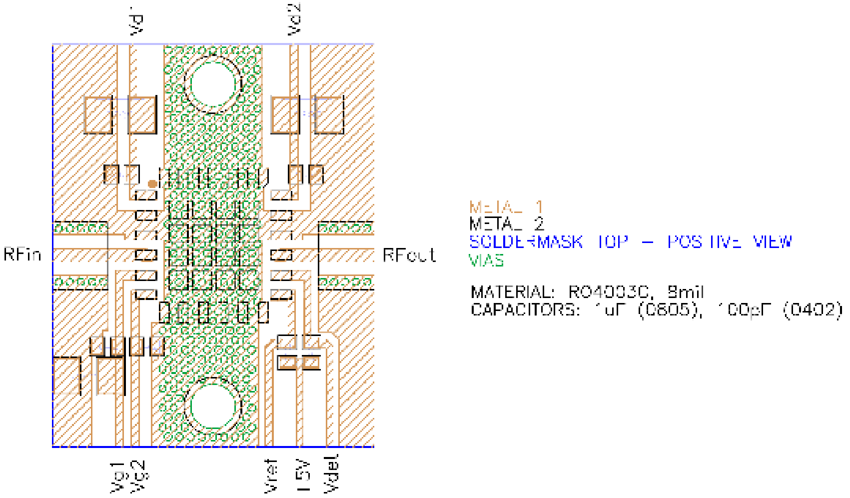
Recommended Layout



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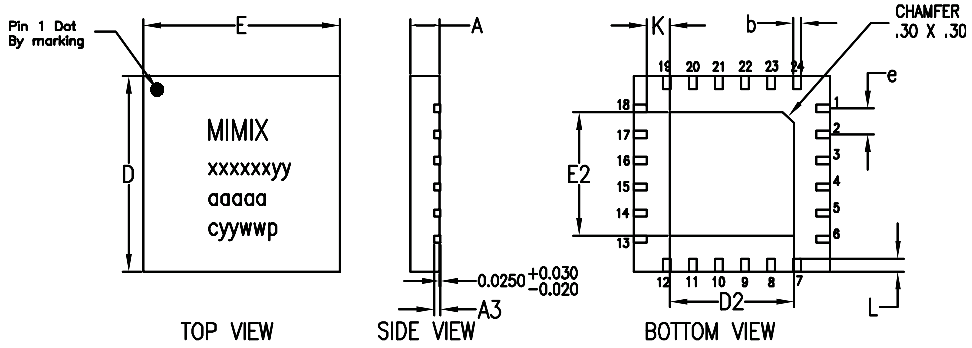
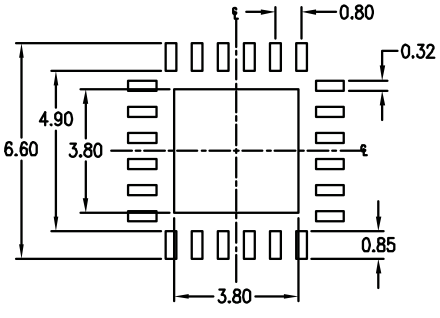
Lead-Free **Package Dimensions/Layout**



MARKINGS:
MIMIX PART/MODEL NO.
WAFER LOT NUMBER
DATE CODE = YYWW
C = COUNTRY OF ORIGIN
P = PLATING OPTION

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
DIMENSIONS ARE IN MM



VIEW IS FROM TOP

NOTES:
1. DIMENSIONS ARE IN MM.

	DIMENSION IN MM		
SYM	MIN	TYP	MAX
A	0.85	0.90	0.95
A3	0.20 REF		
b	0.18	0.23	0.28
K	0.70	–	–
D	6.00 BSC ±0.1		
E	6.00 BSC ±0.1		
e	0.80		
D2	3.70	3.80	3.90
E2	3.70	3.80	3.90
L	0.35	0.40	0.45

1. VIEWS MAY NOT BE TO SCALE: USE DIMENSIONS AND TABLE.
2. MARKINGS ARE FOR ILLUSTRATION PURPOSES ONLY.
ACTUAL MARKINGS MAY VARY FOR EACH DEVICE TYPE.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 1A devices.

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