19-2942; Rev 1; 11/06

可提供评估板

MAXIM

0.5Ω、四路 SPDT 开关，UCSP/QFN 封装

概述

MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A 是低导通电阻模拟开关，采用 +1.8V 至 +5.5V 单电源供电。MAX4754/MAX4754A 和 MAX4755 是双路、双刀双掷(DPDT)开关。MAX4756/MAX4756A 是四路、单刀双掷(SPDT)开关。这些器件可以配置用来切换音频或数据信号。

MAX4754/MAX4754A 有四个 0.5Ω 的 SPDT 开关，用于音频信号切换，并有两个逻辑控制输入。MAX4755 有四个 0.5Ω 的 SPDT 开关(两个开关分别在 NC 端加有额外的 11Ω 串联电阻)。这样用户可以将 8Ω 扬声器当作 32Ω 负载(耳机扬声器)来驱动。MAX4756/MAX4756A 有四个 0.5Ω 的 SPDT 开关，这些开关由一个逻辑控制输入和一个使能输入控制，使能引脚($\overline{EN}$)可用来禁止这些开关。

MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A 提供节省空间的 16 引脚、TQFN 封装和微型、16 焊球、2mm x 2mm 晶片级封装(UCSP™)。

应用

扬声器-耳机开关

音频信号切换

蜂窝电话

PDA/手持式设备

笔记本电脑

UCSP 是 Maxim Integrated Products, Inc.的商标。

引脚配置在数据资料的最后给出。

特性

- 数据与音频信号切换
- 低 R_{ON} (0.5Ω，典型值)音频开关
- 0.1Ω (典型值)通道间匹配度
- 0.2Ω (典型值)导通电阻平坦度
- 0.035% (典型值) THD
- 降低非满摆幅逻辑控制输入情况下的电源电流 (MAX4754A/MAX4756A)
- +1.8V 至 +5.5V 电源范围
- 可处理满摆幅信号
- 16 焊球 UCSP (2mm x 2mm)封装

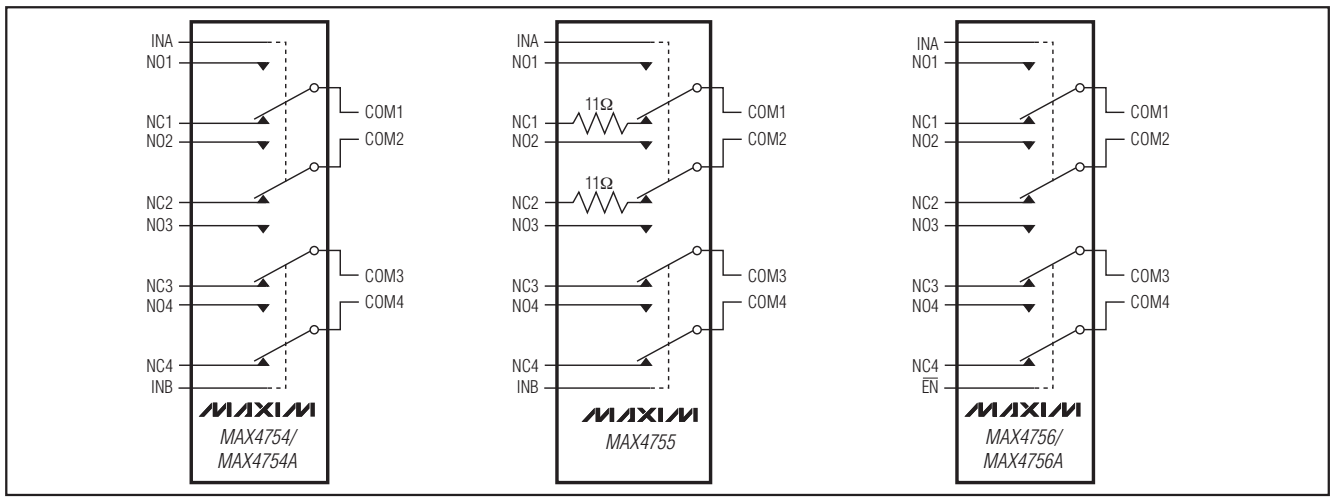
定购信息

PART	PIN-PACKAGE	PKG CODE
MAX4754EBE+T	16 UCSP-16	B16-1
MAX4754ETE+T	16 TQFN-EP**	T1644-4
MAX4754AEBE+T	16 UCSP-16	B16-1
MAX4754AETE+T	16 TQFN-EP**	T1644-4
MAX4755EBE+T*	16 UCSP-16	B16-1
MAX4755ETE+T*	16 TQFN-EP**	T1644-4
MAX4756EBE+T*	16 UCSP-16	B16-1
MAX4756ETE+T*	16 TQFN-EP**	T1644-4
MAX4756AEBE+T*	16 UCSP-16	B16-1
MAX4756AETE+T*	16 TQFN-EP**	T1644-4

***注**：这些器件工作在-40°C 至 +85°C 温度范围。*

** 未来产品—供货情况请联系厂商*
***EP = 裸焊盘。*
+ 表示无铅封装。

功能框图



ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V+, IN_, EN .....-0.3V to +6V
COM_, NO_, NC_ (Note 1) .....-0.3V to (V+ + 0.3V)
Continuous Current
NC1, NC2, COM1, COM2 (MAX4755).....±100mA
NO_, NC_, COM_ (remaining terminal connections) ....±300mA
Peak Current NC1, NC2, COM1, COM2 (MAX4755)
(Pulsed at 1ms, 10% duty cycle).....±200mA
(Pulsed at 1ms, 50% duty cycle).....±150mA
Peak Current NO_, NC_,
COM__ (remaining terminal connections)
(Pulsed at 1ms, 10% duty cycle).....±500mA
(Pulsed at 1ms, 50% duty cycle).....±400mA

Continuous Power Dissipation (T_A = +70°C)
16-Bump UCSP (derate 8.2mW/°C above +70°C) 660mW
16-Pin TQFN (derate 16.9mW/°C above +70°C).....1349mW
ESD per Method 3015.7.....±2kV
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Bump Temperature (soldering)
Infrared (15s) .....+220°C
Vapor Phase (60s) .....+215°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on NO_, NC_, COM_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at +3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$			T_{MIN} to T_{MAX}	0		V+	V
On-Resistance	R_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA, $V_{NC\_}$ or $V_{NO\_}$ = 0V or V+ (Note 4)	MAX4755 (NO1, NO2, N_3, N_4), MAX4754/ MAX4754A/MAX4756/ MAX4756A	+25°C		0.5	0.85	Ω
				T_{MIN} to T_{MAX}			1.0	
			MAX4755 (NC1, NC2)	+25°C		11.5		
				T_{MIN} to T_{MAX}	8.0		12.5	
On-Resistance Match Between Channels	ΔR_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA, $V_{NC\_}$ or $V_{NO\_}$ = +1.5V (Notes 4, 5)	MAX4755 (NO1, NO2, N_3, N_4) MAX4754/ MAX4756/MAX4756A	+25°C		0.1	0.35	Ω
				T_{MIN} to T_{MAX}			0.55	
			MAX4755 (NC1, NC2)	+25°C		0.2	0.4	
				T_{MIN} to T_{MAX}			0.55	
		V+ = +2.7V $I_{COM\_}$ = 10mA, $V_{NC\_}$ or $V_{NO\_}$ = 0 or V+ (Notes 4, 5)	MAX4754A/MAX4756A	+25°C		0.1	0.35	Ω
				T_{MIN} to T_{MAX}			0.55	
On-Resistance Flatness	$R_{FLAT(ON)}$	V+ = 3V, $I_{COM\_}$ = 10mA, $V_{NO\_}$ or $V_{NC\_}$ = 0V, 0.6V, or V+ (Note 6)	MAX4755 (NO1, NO2, N_3, N_4, NO1, NO2), MAX4754/ MAX4754A/MAX4756/ MAX4756A	+25°C		0.2	0.4	Ω
				T_{MIN} to T_{MAX}			0.55	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at +3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
NO_, NC_ Off-Leakage Current	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 3.6V; $V_{COM\_}$ = 3.3V, 0.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A	+25°C	-4		+4	nA
			T_{MIN} to T_{MAX}	-10		+10	
COM_ Off-Leakage Current	$I_{COM\_(OFF)}$	V+ = 3.6V (MAX4756/MAX4756A); $V_{COM\_}$ = 3.3V, 0.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V	+25°C	-6	0.01	+6	Ω
			T_{MIN} to T_{MAX}	-15		+15	
COM_ On-Leakage Current	$I_{COM\_(ON)}$	V+ = 3.6V; $V_{COM\_}$ = 3.3V, 0.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3.3V, 0.3V or unconnected	+25°C	-3		+3	nA
			T_{MIN} to T_{MAX}	-15		+15	
DYNAMIC							
Turn-On Time NC_	$t_{ON, NC}$	V+ = 2.7V, $V_{NC\_}$ = 1.5V, R_L = 50Ω, C_L = 35pF (Figure 1) MAX4754A/MAX4756A	+25°C		320	650	ns
			T_{MIN} to T_{MAX}			900	
Turn-Off Time NC_	$t_{OFF, NC}$	V+ = 2.7V, $V_{NC\_}$ = 1.5V, R_L = 50Ω, C_L = 35pF (Figure 1) MAX4754A/MAX4756A	+25°C		27	60	ns
			T_{MIN} to T_{MAX}			70	
Turn-On Time NO_	$t_{ON, NO}$	V+ = 2.7V, $V_{NC\_}$ = 1.5V, R_L = 50Ω, C_L = 35pF (Figure 1) MAX4754A/MAX4756A	+25°C		70	150	ns
			T_{MIN} to T_{MAX}			200	
Turn-Off Time NO_	$t_{OFF, NO}$	V+ = 2.7V, $V_{NC\_}$ = 1.5V, R_L = 50Ω, C_L = 35pF (Figure 1) MAX4754A/MAX4756A	+25°C		300	650	ns
Turn-On Time	t_{ON}	V+ = 2.7V, $V_{NO\_}$, or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF, (Figure 1) MAX4754/MAX4755/MAX4756	+25°C		45	140	ns
			T_{MIN} to T_{MAX}			150	
Turn-Off Time	t_{OFF}	V+ = 2.7V, $V_{NO\_}$, or $V_{NC\_}$ = 1.5V; R_L = 50Ω; C_L = 35pF (Figure 1) MAX4754/MAX4755/MAX4756	+25°C		25	50	ns
			T_{MIN} to T_{MAX}			60	
Break-Before-Make	t_{BBM}	V+ = 2.7V, $V_{NO\_}$, or $V_{NC\_}$ = 1.5V; R_L = 50Ω, C_L = 35pF (Figure 2) (Note 7)	+25°C		15		ns
			T_{MIN} to T_{MAX}	2			
Charge Injection	Q	V_{GEN} = 0V, R_{GEN} = 0, C_L = 1.0nF (Figure 3)	+25°C		300		pC
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, C_L = 50pF, R_S = 50Ω, R_L = 50Ω	+25°C		10		MHz
Off-Isolation	V_{ISO}	C_L = 5pF, R_L = 50Ω, $V_{COM\_}$ = $1V_{P-P}$ f = 100kHz (Figure 4) (Note 8)	+25°C		-65		dB
Crosstalk	V_{CT}	C_L = 5pF, R_L = 50Ω, $V_{COM\_}$ = $1V_{P-P}$ f = 100kHz (Figure 4) (Note 9)	+25°C		-90		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, $1V_{P-P}$, R_L = 32Ω, V_{DC} = V+/2	+25°C		0.035		%

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +5.25V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at +3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
NO_, NC_ Off-Capacitance	$C_{NO\_(OFF)}$, $C_{NC\_(OFF)}$	V_{NO}, $V_{NC\_}$ = GND, f = 1MHz (Figure 5)	+25°C		180		pF
COM_ Off-Capacitance	$C_{COM\_(OFF)}$	$V_{COM\_}$ = GND, f = 1MHz (Figure 5)	+25°C		300		pF
COM_ On-Capacitance	$C_{(ON)}$	$V_{COM\_}$ = GND, f = 1MHz (Figure 5)	+25°C		400		pF
DIGITAL I/O (IN_, $\overline{EN}$)							
Input Logic-High	V_{IH}	V+ = 2.7V to 3.6V, MAX4754/MAX4755/MAX4756	T_{MIN} to T_{MAX}	1.4			V
		V+ = 2.7V to 5.25V, MAX4754A/MAX4756A	T_{MIN} to T_{MAX}	1.4			
		V+ = 3.6V to 5.25V, MAX4754/MAX4755/MAX4756	T_{MIN} to T_{MAX}	2.0			
Input Logic-Low	V_{IL}	V+ = 2.7V to 3.6V, MAX4754/MAX4755/MAX4756	T_{MIN} to T_{MAX}			0.5	V
		V+ = 2.7V to 5.25V, MAX4754A/MAX4756A	T_{MIN} to T_{MAX}			0.6	
		V+ = 3.6V to 5.25V, MAX4754/MAX4755/MAX4756	T_{MIN} to T_{MAX}			0.5	
Input Leakage Current	I_{IN}	V_{IN} = 0V or V+	T_{MIN} to T_{MAX}			1	µA
POWER SUPPLY							
Power-Supply Range	V+		T_{MIN} to T_{MAX}	1.8		5.5	V
Power-Supply Current	I+	V+ = 5.5V, $V_{IN\_}$ = 0V or V+, MAX4754/MAX4754A/MAX4755/MAX4756	+25°C		0.2		µA
			T_{MIN} to T_{MAX}			2	
		V+ = 5.5V, $V_{IN\_}$ = 0.5V or 1.4V, MAX4754A/MAX4756A	+25°C		6.5		µA
			T_{MIN} to T_{MAX}			12	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: UCSP parts are 100% tested at +25°C and limits across the full temperature range are guaranteed by correlation and design. TQFN parts are 100% tested at +85°C and limits across the full temperature range are guaranteed by correlation and design.

Note 4: R_{ON} and ΔR_{ON} matching specifications are guaranteed by design and correlation.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Guaranteed by design, not production tested.

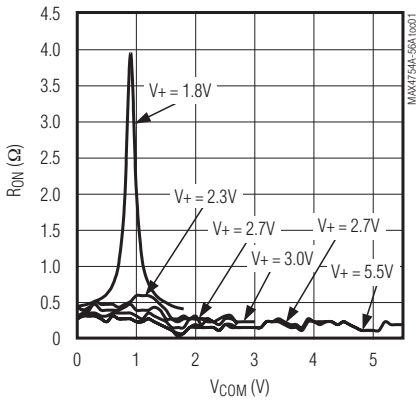
Note 8: Off-Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})], V_{COM} = output, V_{NO} or V_{NC} = input to off switch.

Note 9: Between any two switches.

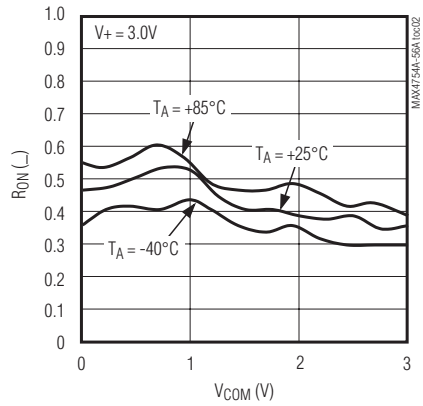
典型工作特性

(V+ = 3V, T_A = +25°C, unless otherwise noted.)

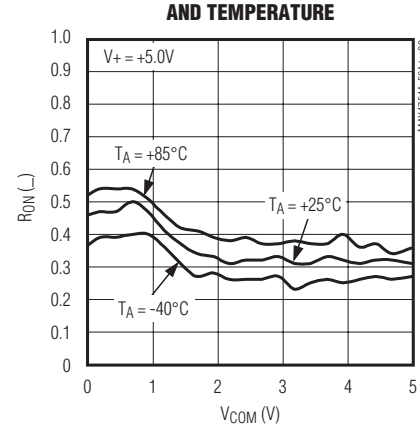
ON-RESISTANCE vs. V_{COM} (MAX4754A/MAX4756A)



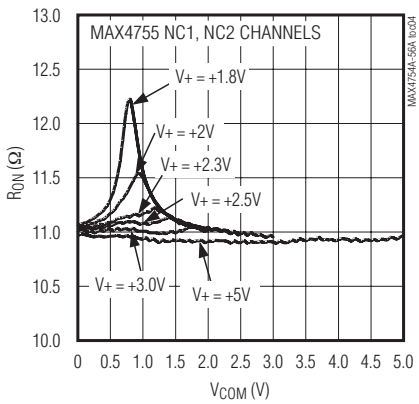
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



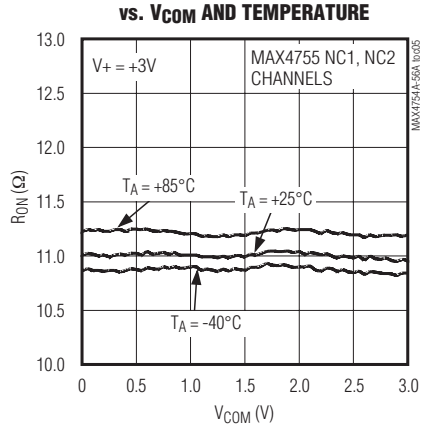
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



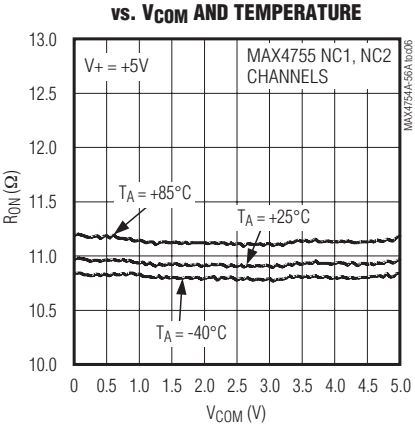
ON-RESISTANCE vs. V_{COM}



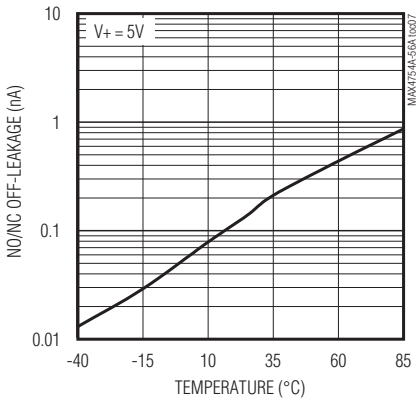
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



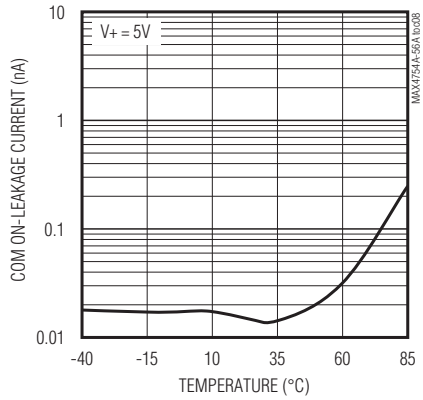
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



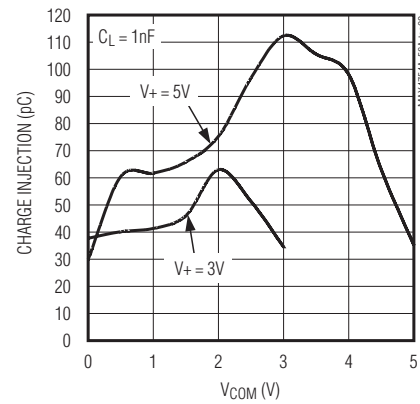
NO/NC OFF-LEAKAGE CURRENT vs. TEMPERATURE (MAX4754/MAX4755/MAX4756)



COM ON-LEAKAGE CURRENT vs. TEMPERATURE



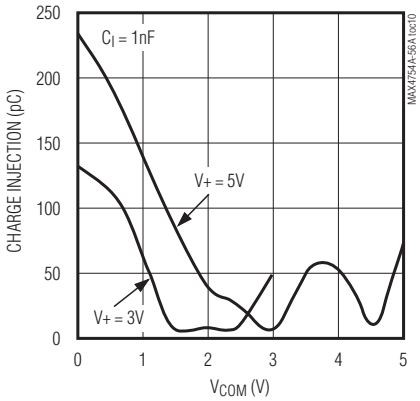
CHARGE INJECTION vs. V_{COM} (MAX4754/MAX4755/MAX4756)



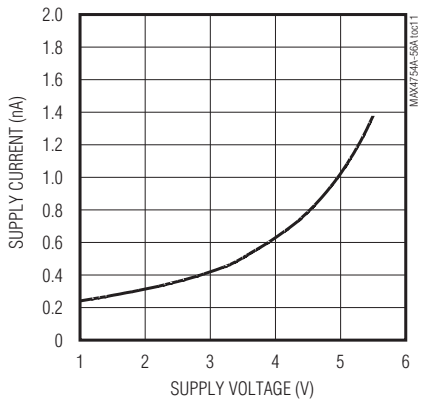
典型工作特性(续)

(V+ = 3V, T_A = +25°C, unless otherwise noted.)

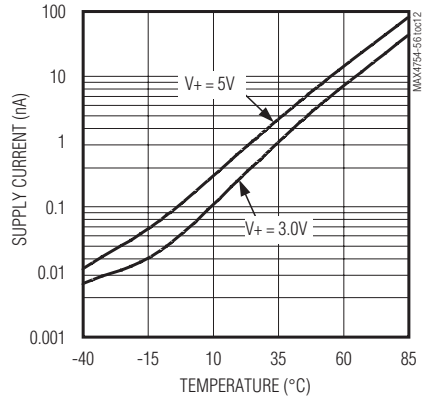
CHARGE INJECTION vs. V_{COM}



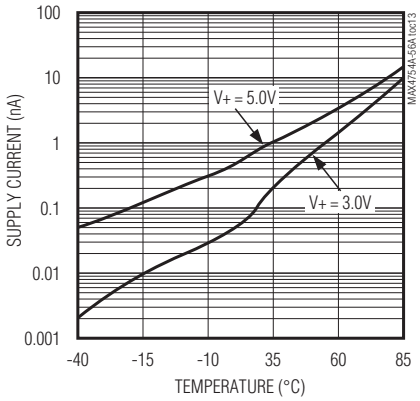
SUPPLY CURRENT vs. SUPPLY VOLTAGE



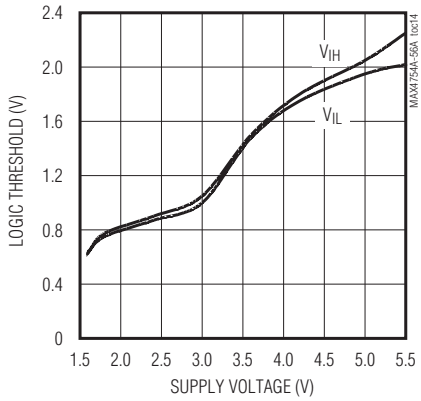
SUPPLY CURRENT vs. TEMPERATURE (MAX4754/MAX4755/MAX4756)



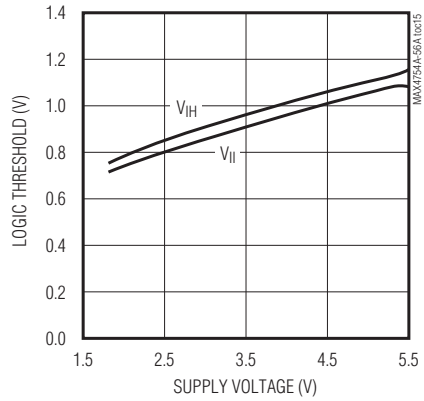
SUPPLY CURRENT vs. TEMPERATURE (MAX4754A/MAX4756A)



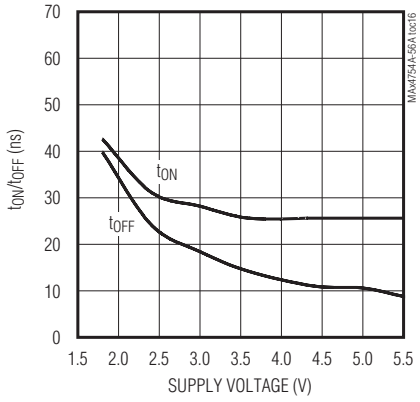
LOGIC THRESHOLD vs. SUPPLY VOLTAGE (MAX4754/MAX4755/MAX4756)



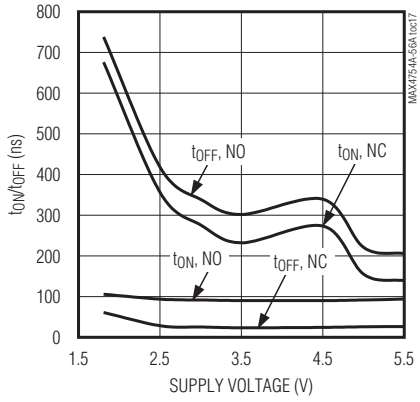
LOGIC THRESHOLD vs. SUPPLY VOLTAGE (MAX4754A/MAX4756A)



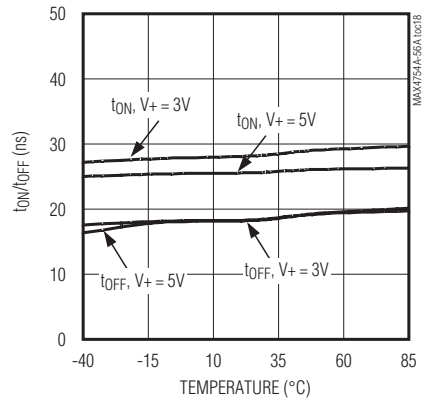
TURN-ON/OFF TIMES vs. SUPPLY VOLTAGE (MAX4754/MAX4755/MAX4756)



TURN-ON/OFF TIMES vs. SUPPLY VOLTAGE (MAX4754A)



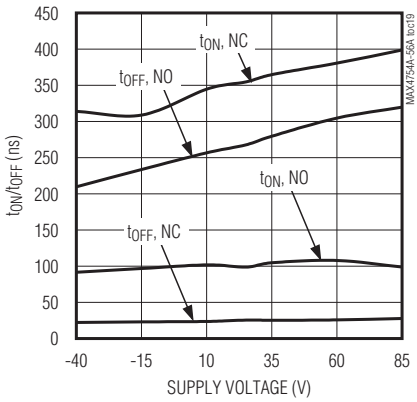
TURN-ON/OFF TIMES vs. TEMPERATURE (MAX4754/MAX4755/MAX4756)



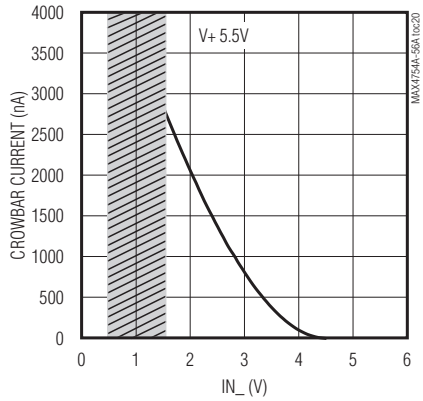
典型工作特性(续)

(V+ = 3V, T_A = +25°C, unless otherwise noted.)

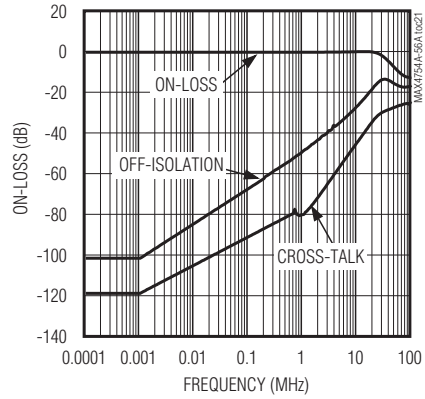
TURN-ON/OFF TIMES vs. TEMPERATURE (MAX4754A)



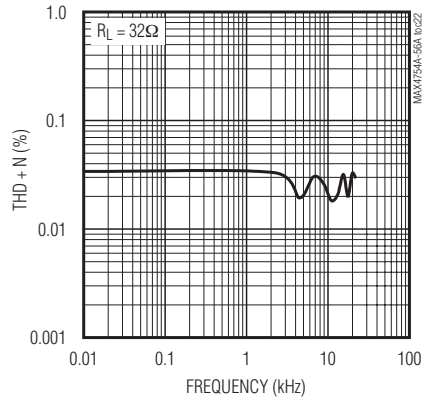
SUPPLY CURRENT vs. LOGIC CONTROL INPUT



FREQUENCY REPSONSE



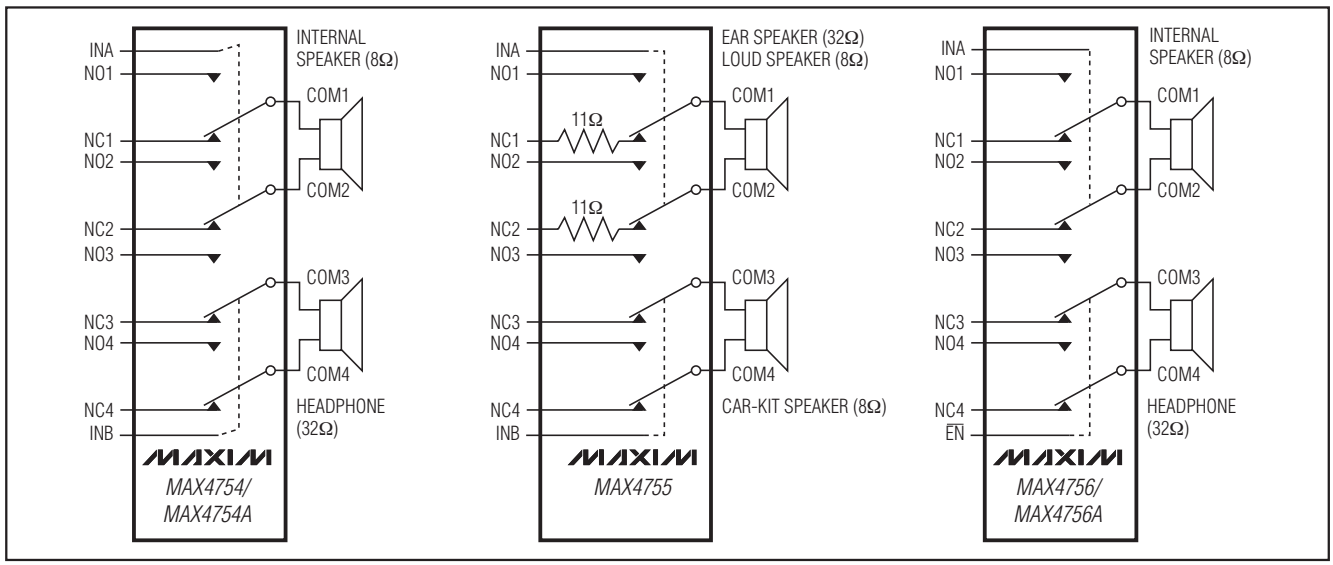
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



引脚说明

引脚						名称	功能
MAX4754/MAX4754A		MAX4755		MAX4756/MAX4756A			
UCSP	QFN	UCSP	QFN	UCSP	QFN		
C1	1	C1	1	C1	1	NO1	模拟开关 1，常开端 1。
C2	2	C2	2	C2	2	INA	开关 1 和 2 的逻辑控制数字输入。MAX4756 中开关 1–4 的数控输入。
B1	3	B1	3	B1	3	COM1	模拟开关 1，公共端 1。
A1	4	A1	4	A1	4	NC1	模拟开关 1，常闭端 1。
A2	5	A2	5	A2	5	NO4	模拟开关 4，常开端 4。
B2	6	B2	6	B2	6	V+	正电源输入。
A3	7	A3	7	A3	7	COM4	模拟开关 4，公共端 4。
A4	8	A4	8	A4	8	NC4	模拟开关 4，常闭端 4。
B4	9	B4	9	B4	9	NO2	模拟开关 2，常开端 2。
B3	10	B3	10	—	—	INB	开关 3 和 4 的逻辑控制数字输入
—	—	—	—	B3	10	$\overline{EN}$	输出使能，低电平有效。
C4	11	C4	11	C4	11	COM2	模拟开关 2，公共端 2。
D4	12	D4	12	D4	12	NC2	模拟开关 2，常闭端 2。
D3	13	D3	13	D3	13	NO3	模拟开关 3，常开端 3。
C3	14	C3	14	C3	14	GND	地。
D2	15	D2	15	D2	15	COM3	模拟开关 3，公共端 3。
D1	16	D1	16	D1	16	NC3	模拟开关 3，常闭端 3。
—	EP	—	EP	—	EP	EP	裸露焊盘，将 EP 与 GND 相连。

典型工作电路



详细说明

MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A 是低导通电阻模拟开关，采用 +1.8V 至 +5.5V 单电源供电。这些器件完全规范于电源标称值为 3V 的应用。

MAX4754/MAX4754A DPDT 开关有两个逻辑控制输入，每个输入控制两个 SPDT 开关。每个开关的 NO 和 NC 端的导通电阻为 0.5Ω，这使其非常适合音频信号切换。

MAX4755 DPDT 开关也有四个 0.5Ω 的 SPDT 开关，开关 1 和 2 的 NC 端还加有 11.5Ω 的串联电阻。该特性允许用户将 8Ω 扬声器当作 32Ω 负载来驱动，使之可以作为耳机扬声器来使用。使用两个逻辑控制输入控制四个开关。

MAX4756/MAX4756A 有四个 0.5Ω 的 SPDT 开关，由一个逻辑控制输入(INA)和一个 $\overline{EN}$ 输入来控制，$\overline{EN}$ 输入用来禁止开关。

应用信息

数控输入

无论采用何种电源电压，MAX4754/MAX4754A/MAX4755/MAX4756/MAX4756A 的逻辑输入端都可以承受最大 +5.5V 的电压。例如在 +3.3V 供电时，IN_ 端可以低至 GND，也可以高至 +5.5V，这就允许混合逻辑电平共存于同一个系统中。满摆幅驱动控制逻辑输入可将功耗降至最低。在 +3V 电源电压下，逻辑电平门限值为 0.5V (低)和 1.4V (高)。

对于 MAX4756/MAX4756A，将 $\overline{EN}$ 驱动至低电平使能 COM_。当 $\overline{EN}$ 为高电平时，COM_ 为高阻状态。

模拟信号电平

整个供电电压范围内(0V 到 V+)的模拟信号输入都可通过开关，且导通电阻变化极小(见*典型工作特性*)。开关是双向的，因此 NO_、NC_ 和 COM_ 既可作为输入也可作为输出。

电源旁路

电源旁路能够改善噪声容限，并能阻止开关噪声从 V+ 电源传播到其他器件。在 V+ 和 GND 之间连接一个 0.1µF 电容即可满足大多数应用的要求。

UCSP 应用信息

关于 UCSP 结构、尺寸、载带信息、印刷电路板技术、焊盘布局、推荐的回流焊温度特性，以及可靠性测试结果的最新应用数据，可从 Maxim 网站 www.maxim-ic.com.cn/ucsp 下载应用笔记：*UCSP—晶片级封装*。

测试电路/时序图

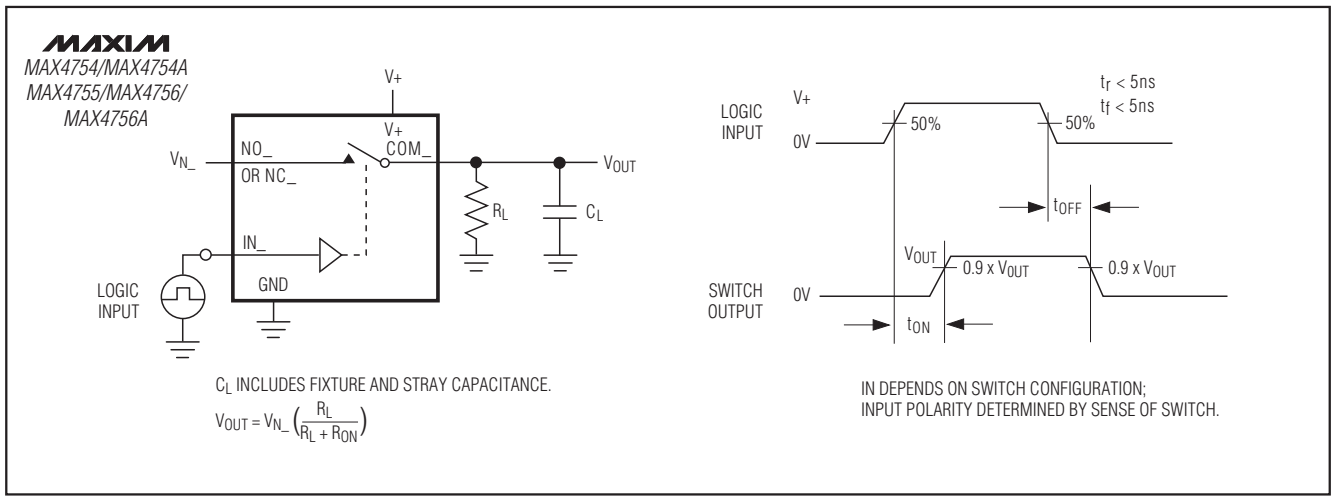


图1. 开关时间

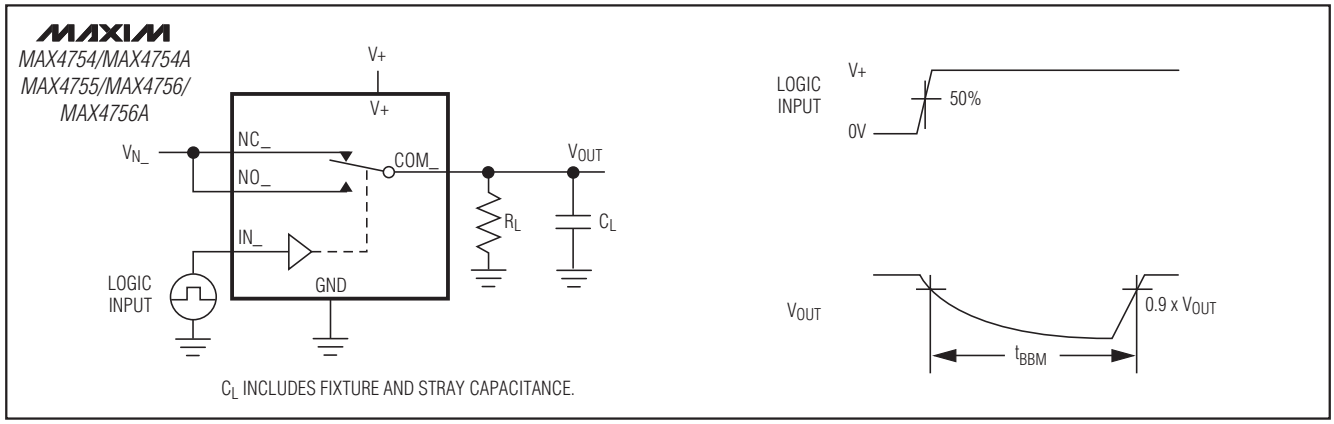


图2. 先断后合的间隔

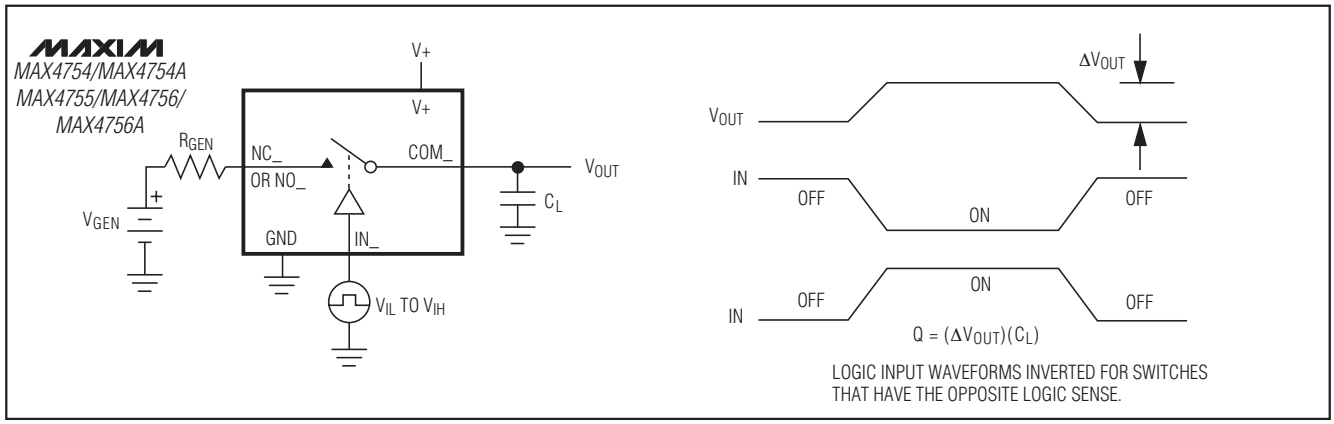


图3. 电荷注入

测试电路/时序图(续)

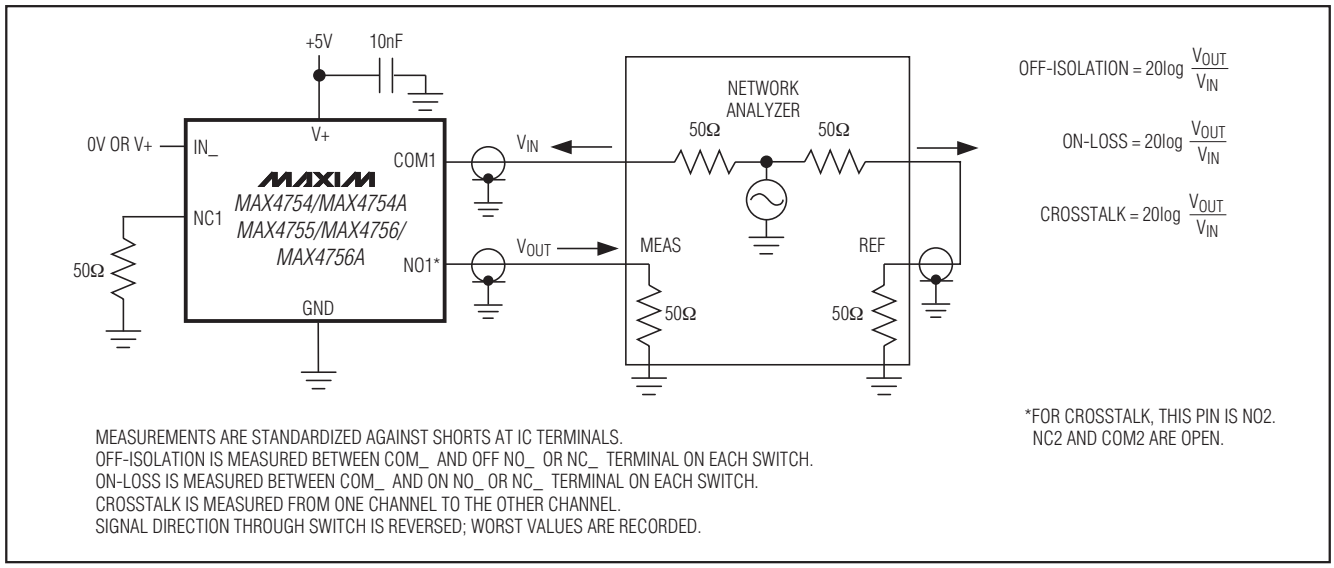


图4. 导通损耗、关断隔离和串扰

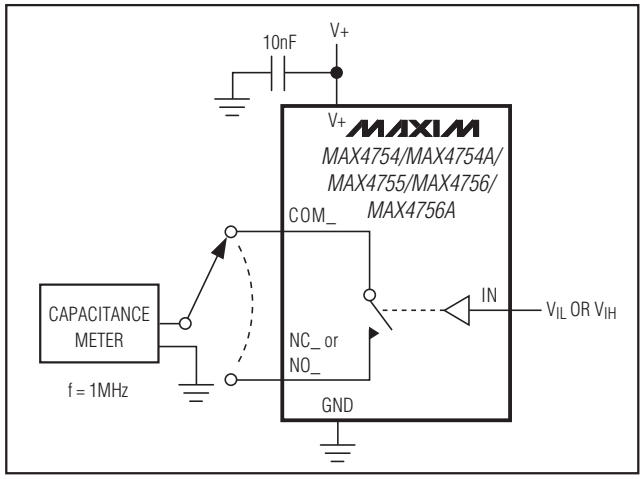


图5. 通道开/关电容

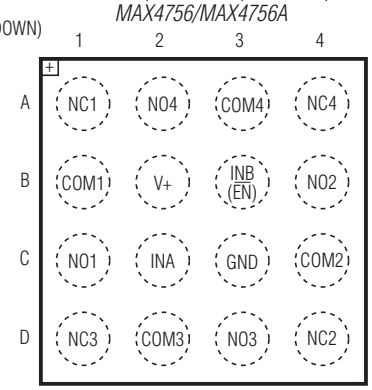
引脚配置/真值表

TOP VIEW

MAXIM

MAX4754/MAX4754A/MAX4755/
MAX4756/MAX4756A

(BUMP SIDE DOWN)

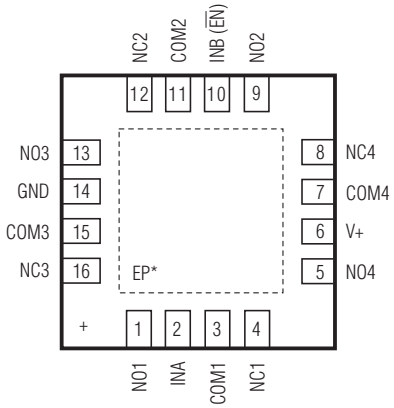


( ) FOR MAX4756/MAX4756A.

UCSP

MAXIM

MAX4754
MAX4754A
MAX4755
MAX4756
MAX4756A



TQFN

***EP:** EXPOSED PADDLE CONNECTED TO GND.

MAX4754/MAX4754A/MAX4755

INA	NO1/NO2	NC1/NC2	NO3/NO4	NC3/NC4
LOW	OFF	ON	—	—
HIGH	ON	OFF	—	—
INB				
LOW	—	—	OFF	ON
HIGH	—	—	ON	OFF

MAX4756/MAX4756A

$\overline{EN}$	INA	NO_	NC_
LOW	LOW	OFF	ON
LOW	HIGH	ON	OFF
HIGH	X	OFF	OFF
HIGH	X	OFF	OFF

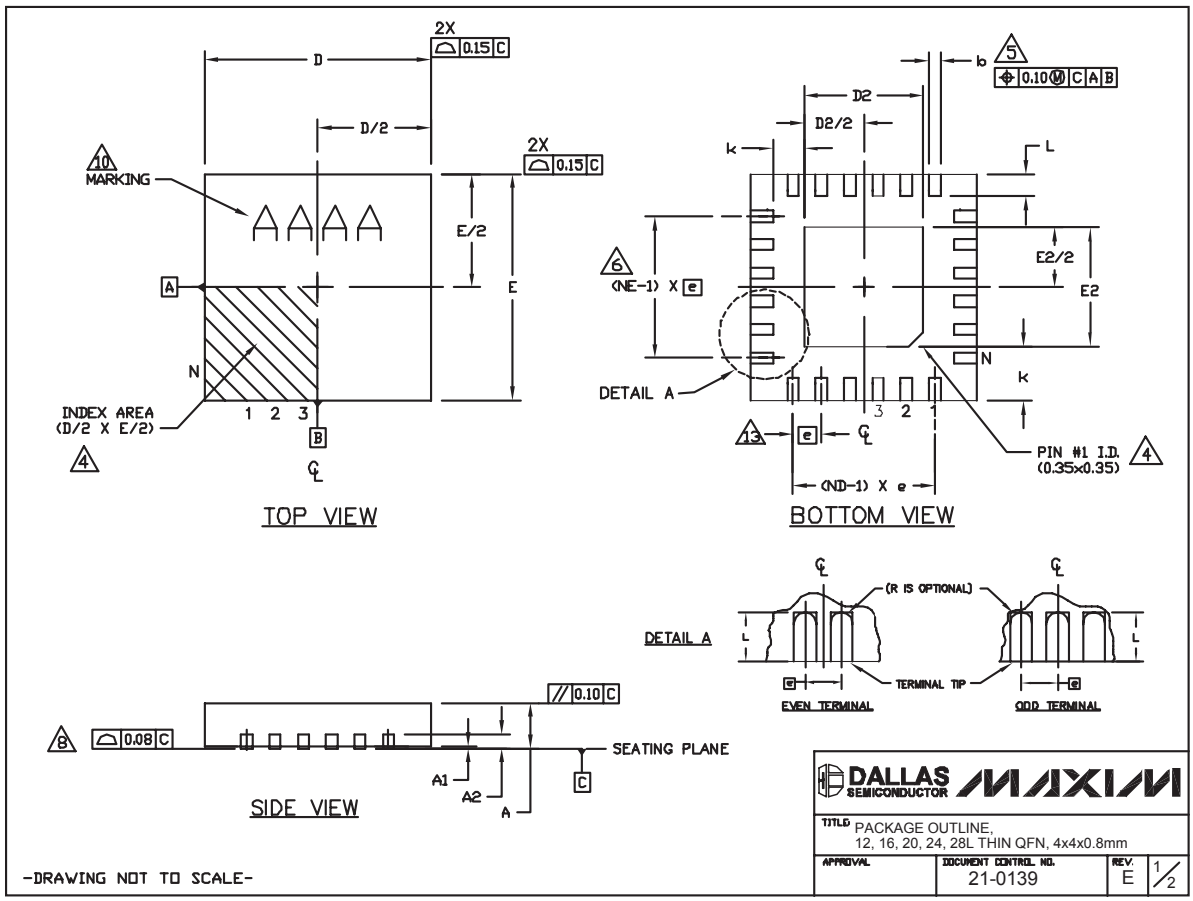
芯片信息

PROCESS: CMOS

封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外形信息，请查询 **www.maxim-ic.com.cn/packages**。)

24L QFN THIN.EPS



封装信息(续)

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外形信息，请查询 **www.maxim-ic.com.cn/packages**。)

COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	E	2/2

封装信息(续)

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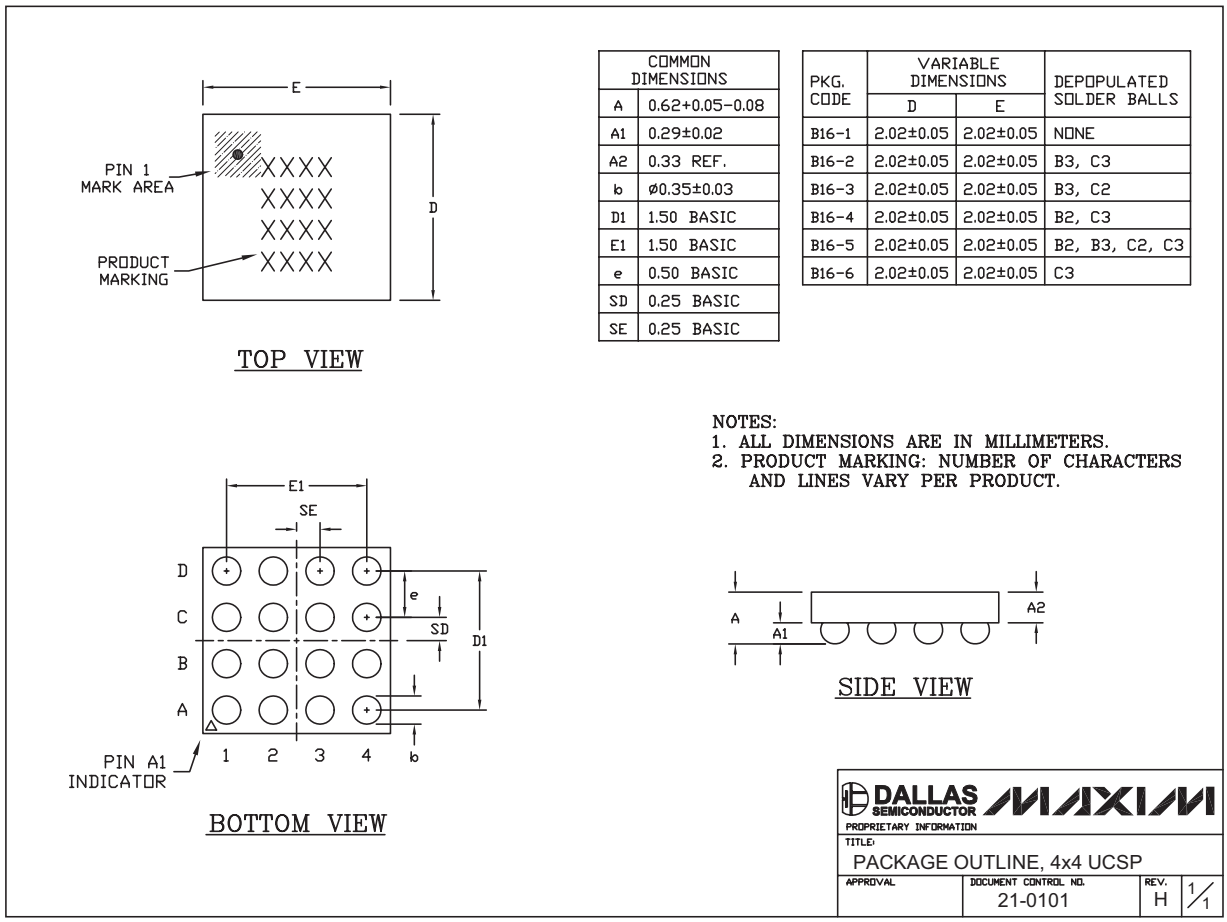
16L,UCSP.EPS



COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.50 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B16-1	2.02±0.05	2.02±0.05	NONE
B16-2	2.02±0.05	2.02±0.05	B3, C3
B16-3	2.02±0.05	2.02±0.05	B3, C2
B16-4	2.02±0.05	2.02±0.05	B2, C3
B16-5	2.02±0.05	2.02±0.05	B2, B3, C2, C3
B16-6	2.02±0.05	2.02±0.05	C3

修订历史

Rev 1 中的修改页：1–5、7、8、13、14、15。

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