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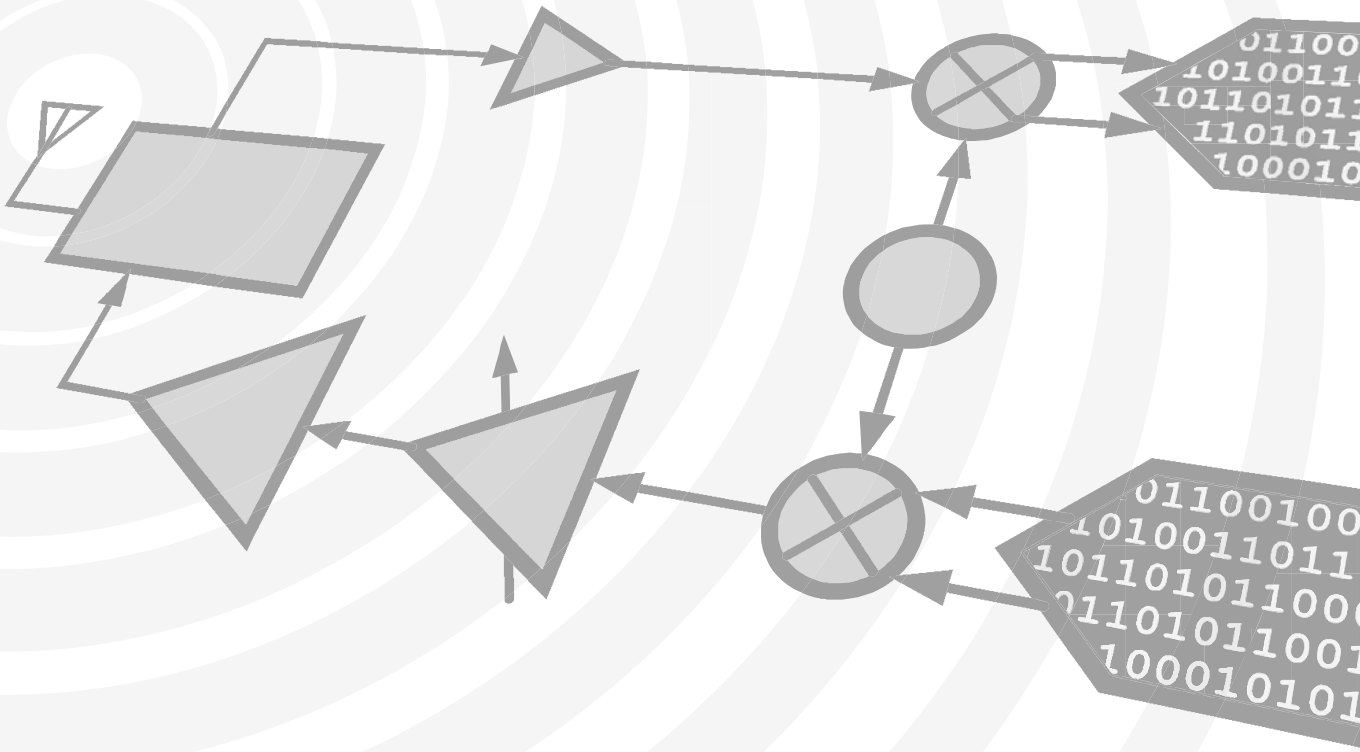

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# HMC1087

## 8 WATT GaN MMIC POWER AMPLIFIER, 2 - 20 GHz



### Typical Applications

The HMC1087 is ideal for:

- Test Instrumentation
- General Communications
- Radar

### Features

High Psat: +39 dBm

Power Gain at Psat: +5.5 dB

High Output IP3: +44 dBm

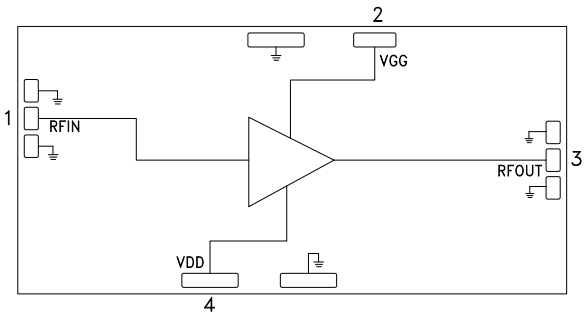
Small Signal Gain: 11 dB

Supply Voltage: +28 V @ 850 mA

50 Ohm Matched Input/Output

Die Size: 2 x 4 x 0.1 mm

### Functional Diagram




### General Description

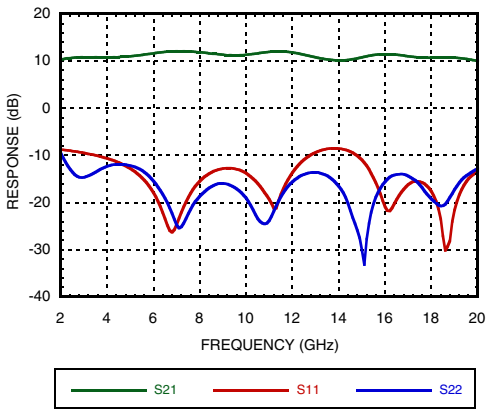
The HMC1087 is an 8W Gallium Nitride (GaN) MMIC Power Amplifier which operates between 2 and 20 GHz. The amplifier typically provides 11dB of small signal gain, +39 dBm of saturated output power, and +44 dBm output IP3 at +29 dBm output power per tone. The HMC1087 draws 850 mA quiescent current from a +28V DC supply. The RF I/Os are matched to 50 Ohms for ease of integration into Multi-Chip-Modules (MCMs). All electrical performance data was acquired with the die eutectically attached to 1.02 mm (40 mil) thick CuMo carrier with multiple 1.0 mil diameter ball bonds connecting the die to 50 Ohm transmission lines on alumina.

### Electrical Specifications, Tc = +25°C, Vdd = +28 V, Idd = 850 mA [1]

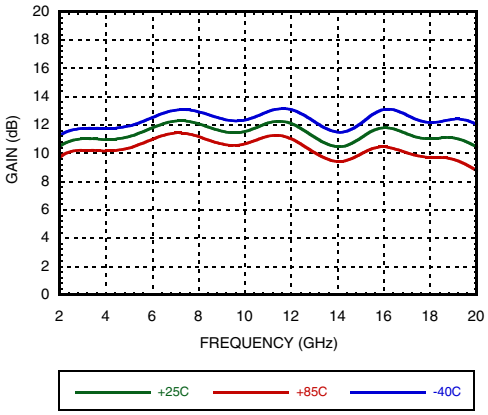
| Parameter | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Frequency Range | | 2 - 6 | | | 6 - 18 | | | 18 - 20 | | GHz |
| Small Signal Gain | 10 | 11 | | 10 | 12 | | 10 | 12 | | dB |
| Gain Flatness | | ±0.5 | | | ±1.0 | | | ±0.5 | | dB |
| Gain Variation Over Temperature | | 0.012 | | | 0.016 | | | 0.024 | | dB/ °C |
| Input Return Loss | | 8 | | | 8 | | | 15 | | dB |
| Output Return Loss | | 10 | | | 12 | | | 12 | | dB |
| Output Power for 3 dB Compression (P3dB) | | 38 | | | 38 | | | 38 | | dBm |
| Power Gain for 3 dB compression (P3dB) | | 8.5 | | | 8.5 | | | 8 | | dB |
| Saturated Output Power (Psat) | | 39 | | | 40 | | | 39 | | dBm |
| Output Third Order Intercept (IP3) [2] | | 44 | | | 44 | | | 43.5 | | dBm |
| Power Added Efficiency | | 24 | | | 22 | | | 20 | | % |
| Quiescent Supply Current (Idd @ Vdd = 28V) | | 850 | | | 850 | | | 850 | | mA |

*[1] Assumes eutectic attach of die to a 40mil CuMo carrier, and 25°C is maintained at the back of the carrie*
*[2] Measurement taken at Pout / tone = +29 dBm*

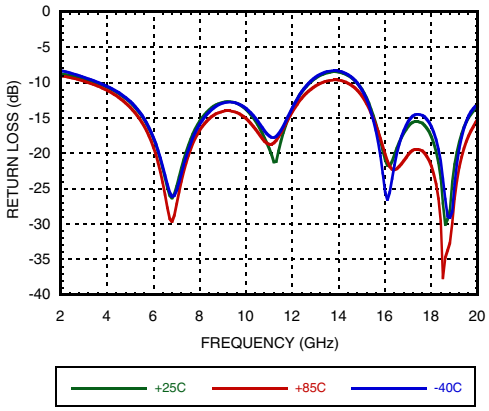
### Gain and Return Loss



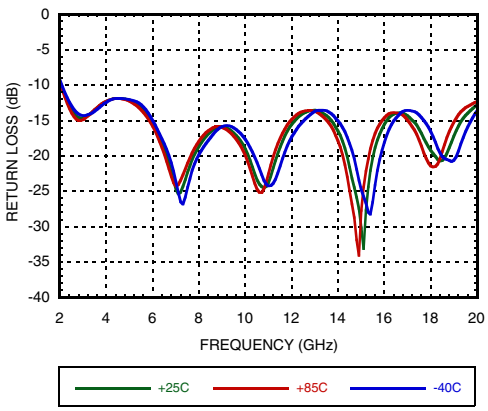

### Gain vs. Temperature



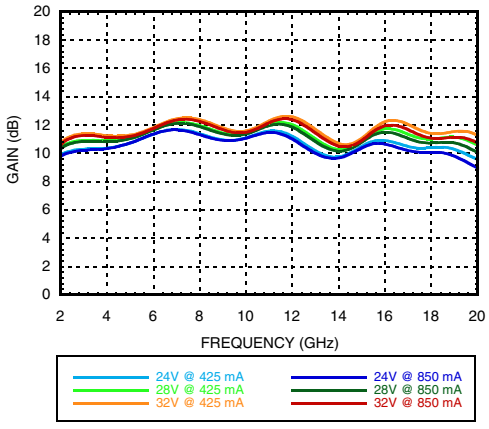

### Input Return Loss vs. Temperature



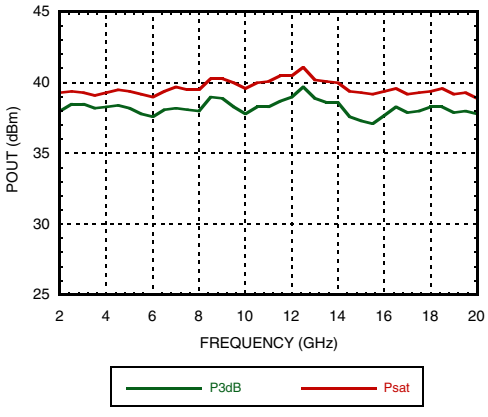

### Output Return Loss vs. Temperature



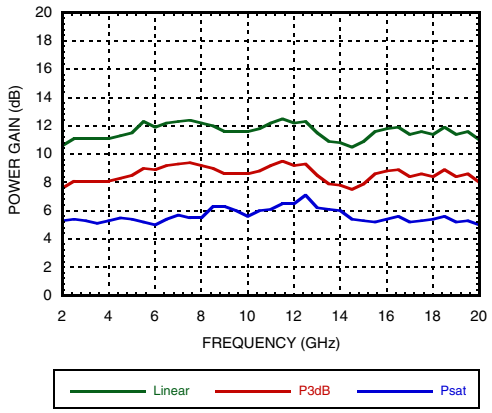

### Gain vs. Bias



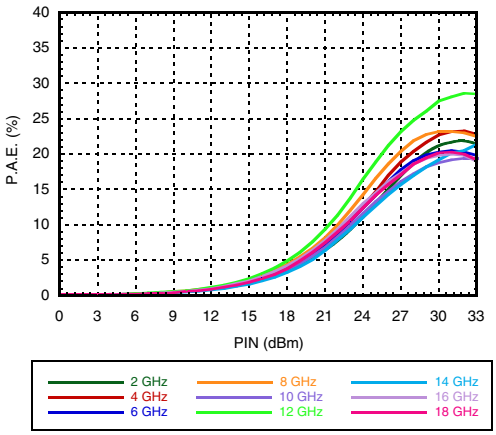

### P3dB vs. Frequency



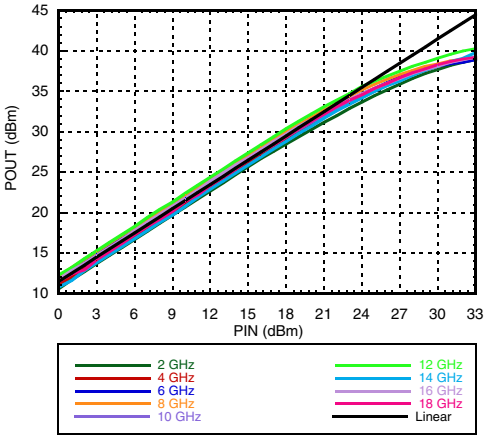
### Power Gain vs. Frequency



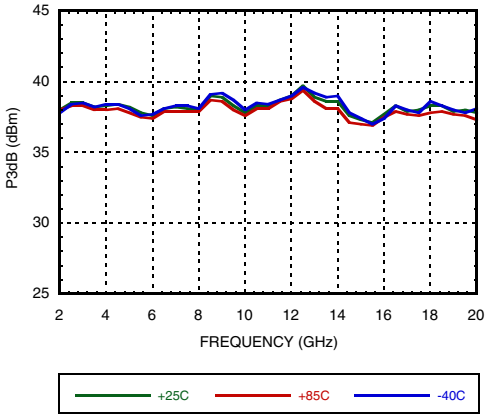

### Power Added Efficiency vs. Pin



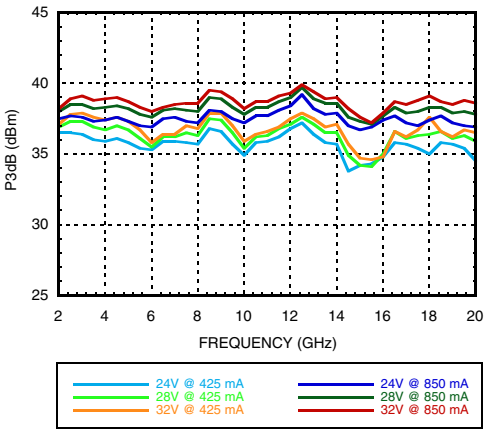

### Pout vs. Pin



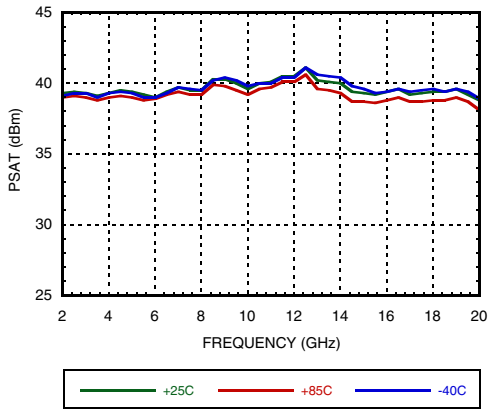

### P3dB vs. Temperature



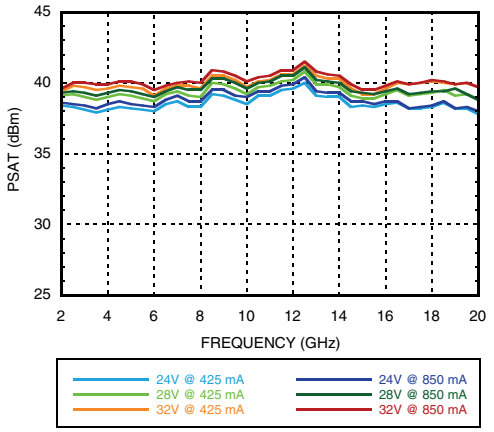

### P3dB vs. DC Bias



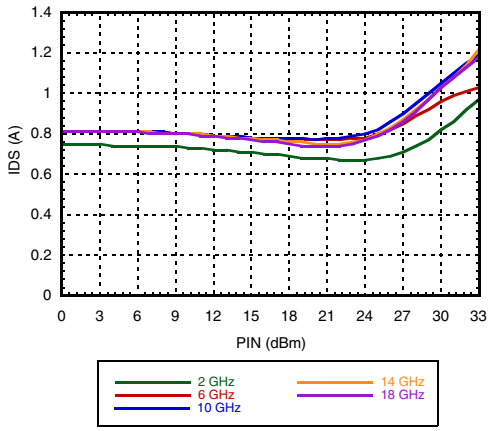

### Psat vs. Temperature



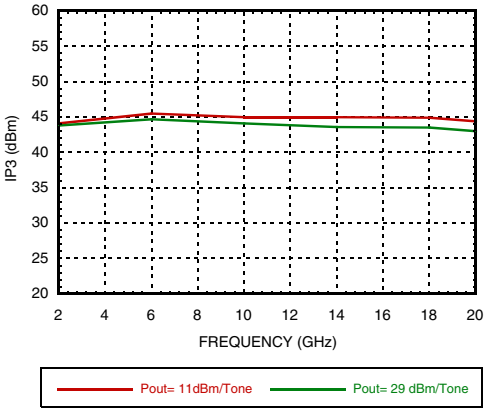
### Psat vs. DC Bias



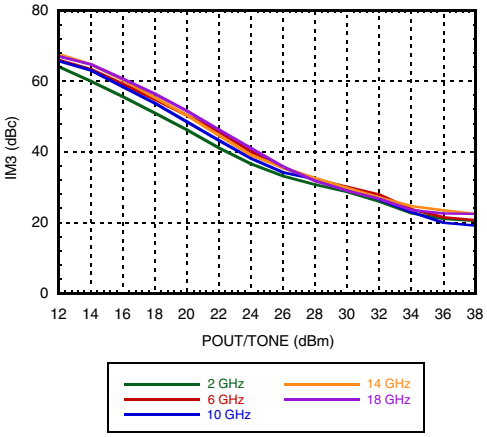

### IDS vs. Pin



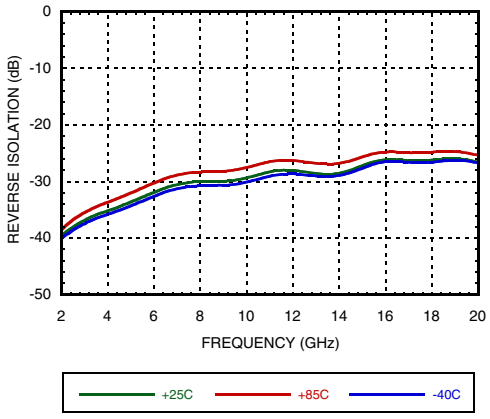

### OIP3 vs. Frequency



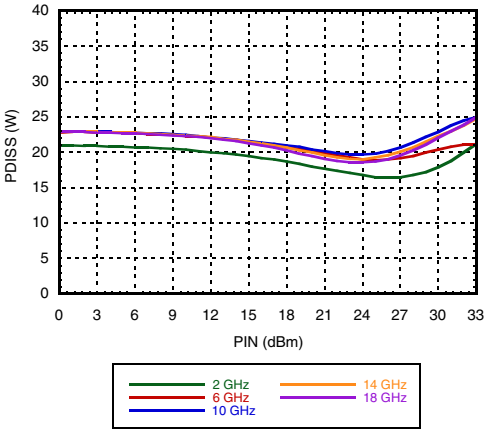

### IM3 vs. Pout/Tone



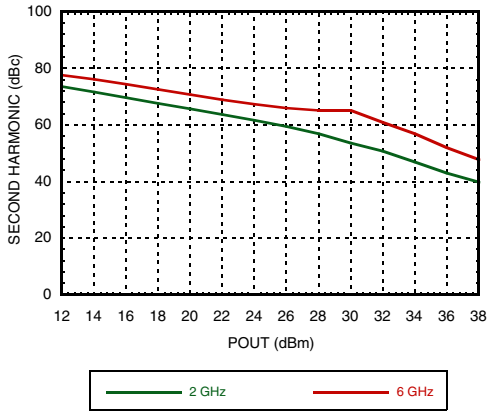

### Reverse Isolation vs. Temperature




### Power Dissipation vs. Pin



### Second Harmonic



## Absolute Maximum Ratings[1]

| | |
|---|---|
| Drain Bias Voltage (Vdd) | +32V |
| Gate Bias Voltage (Vgg) | -8V to +0V |
| Maximum Forward Gate Current | 4 mA |
| Maximum RF Input Power (RFIN) | 34 dBm |
| Maximum Junction Temperature (Tj) | 225 °C |
| Maximum Pdiss (T=85°C) (Derate 236 mW/°C above 85°C) | 33 W |
| Thermal Resistance [2] | 4.24 °C/W |
| Maximum VSWR [3] | 4:1 |
| Storage Temperature | -55 to +150 °C |
| Operating Temperature | -40 to +85 °C |

## Typical Supply Current vs. Vdd

| Vdd (V) | Idd (mA) |
|---|---|
| +28.0 | 850 |

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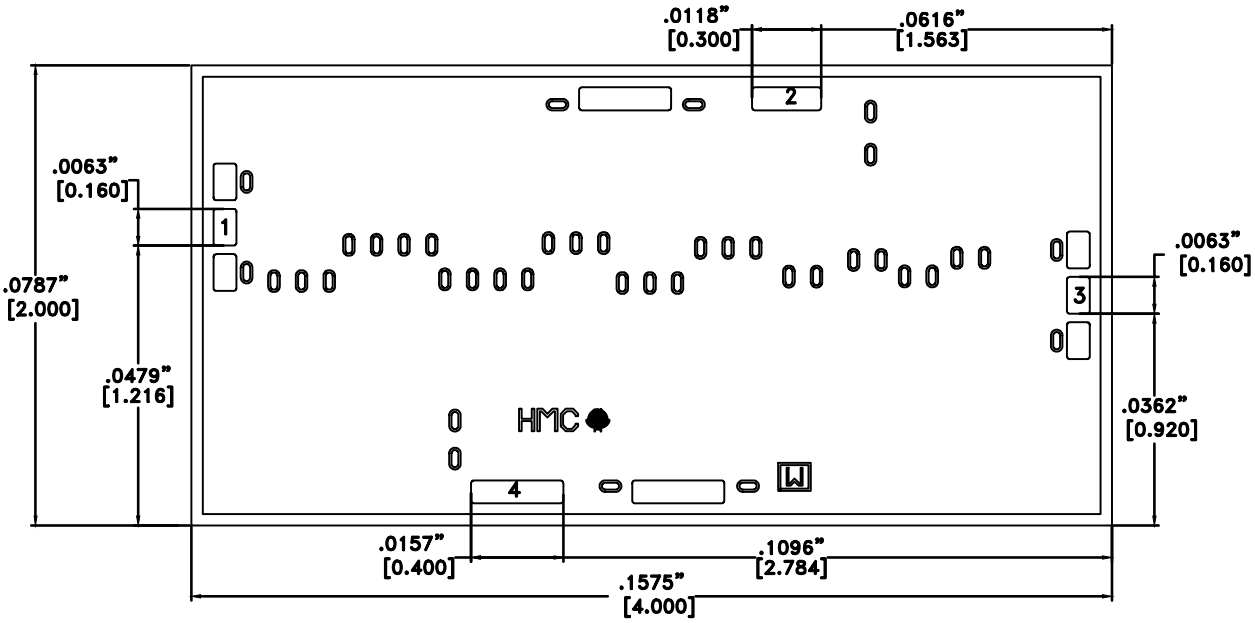
*[1] Operation outside parameter ranges above can cause permanent damage to the device. These are maximum stress ratings only. Continuous operation of the device at these conditions is not implied.*
*[2] Assumes 0.5mil AuSn die attach to a 40mil CuMo Carrier with 85°C at the back of the carrier.*
*[3] Restricted by maximum power dissipation*

## Outline Drawing



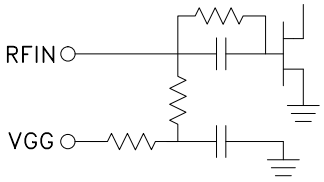
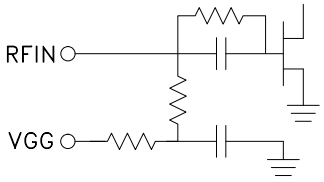
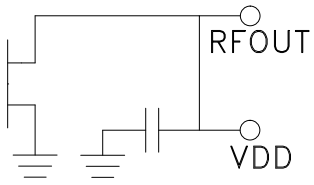
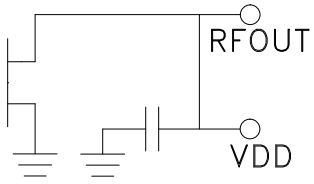

NOTES:
1. ALL DIMENSIONS ARE IN INCHES [MM]
2. DIE THICKNESS IS .004"
3. TYPICAL BOND PAD IS .004" SQUARE
4. BACKSIDE METALLIZATION: GOLD
5. BOND PAD METALLIZATION: GOLD
6. BACKSIDE METAL IS GROUND.
7. CONNECTION NOT REQUIRED FOR UNLABELED BOND PADS.
8. OVERALL DIE SIZE ± .002

## Die Packaging Information [1]

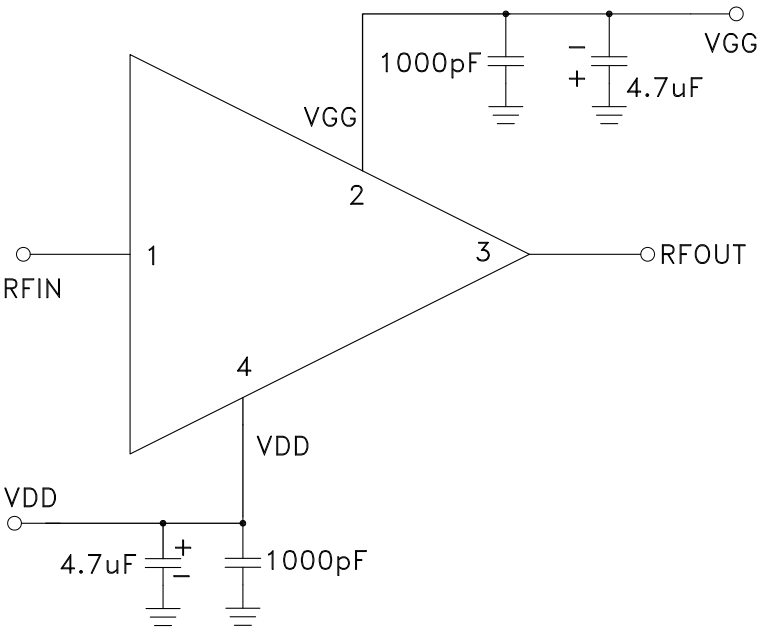
| Standard | Alternate |
|---|---|
| GP-1 (Gel Pack) | [2] |

*[1] Refer to the "Packaging Information" section for die packaging dimensions.*
*[2] For alternate packaging information contact Hittite Microwave Corporation.*

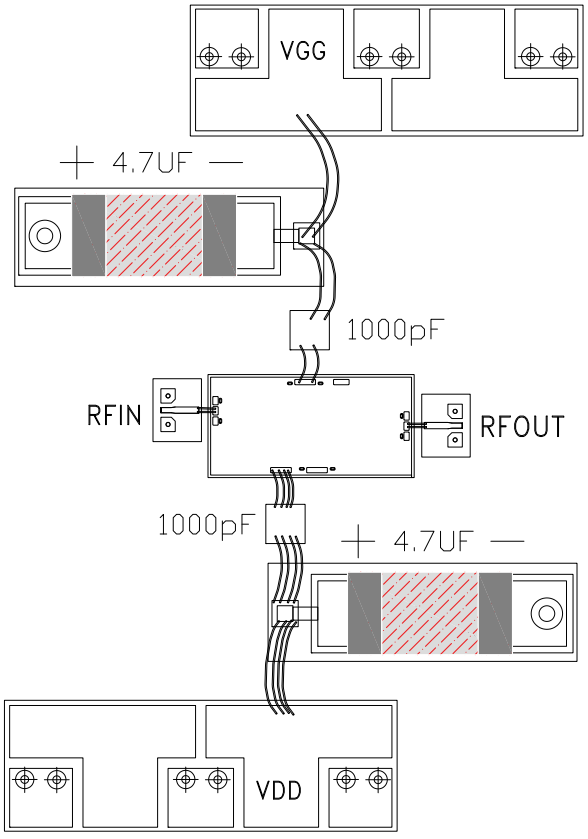
### Pad Descriptions

| Pad Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1 | RFIN | This pad is DC coupled and is matched to 50 Ohms. External blocking capacitor is required |   |
| 2 | VGG | Gate Bias (Internally isolated from RFIN) |   |
| 3 | RFOUT | This pad is DC coupled and is matched to 50 Ohms. External blocking capacitor is required. |   |
| 4 | VDD | Drain Bias (Internally isolated from RFOUT) |   |
| Die Bottom | GND | Die bottom must be connected to RF/DC ground. | |

### Application Circuit




### Assembly Diagram



### Mounting & Bonding Techniques for GaN MMICs

The die should be eutectically attached directly to the ground plane (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a copper tungsten or CuMo heat spreader which is then attached to the thermally conductive ground plane (Figure 2).

Microstrip substrates should be placed as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm to 0.152 mm (3 to 6 mils).

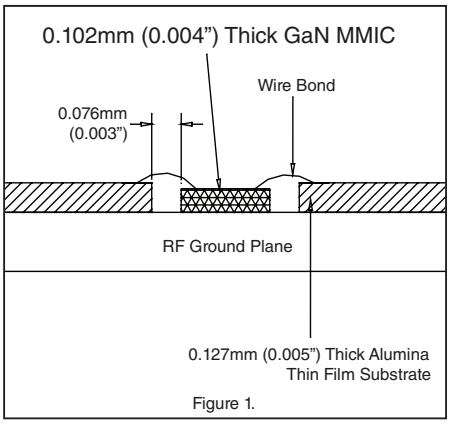



Figure 1.

### Handling Precautions

Follow these precautions to avoid permanent damage.

**Storage:** All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

**Cleanliness:** Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

**Static Sensitivity:** Follow ESD precautions to protect against ESD strikes.

**Transients:** Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

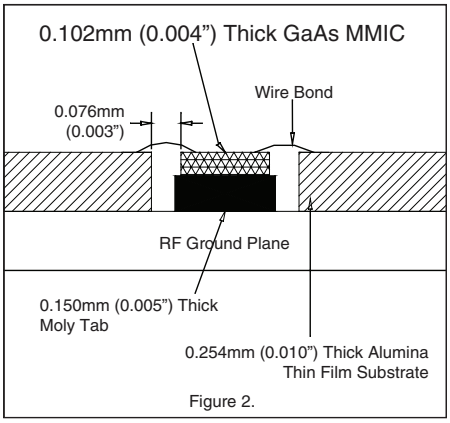



Figure 2.

**Die placement:** A heated vacuum collet (180°C) is the preferred method of pick up. Ensure that the area of vacuum contact on the die is minimized to prevent cracking under differential pressure. All air bridges (if applicable) must be avoided during placement. Minimize impact forces applied to the die during auto-placement.

### Mounting

The chip is back-metallized with a minimum of 5 microns of gold and is the RF ground and thermal interface. It is recommended that the chip be die mounted with AuSn eutectic preforms. The mounting surface should be clean and flat.

**Eutectic Reflow Process:** An 80/20 gold tin 0.5mil (13um) thick preform is recommended with a work surface temperature of 280°C. Limit exposure to temperatures above 300°C to 30 seconds maximum. A die bonder or furnace with 95% $N_2$ / 5% $H_2$ reducing atmosphere should be used. No organic flux should be used. Coefficient of thermal expansion matching is critical for long term reliability.

**Die Attach Inspection:** X-ray or acoustic scan is recommended.

### Wire Bonding

Thermosonic ball or wedge bonding is the preferred interconnect technique. Gold wire must be used in a diameter appropriate for the pad size and number of bonds applied. Force, time and ultrasonics are critical parameters: optimize for a repeatable, high bond pull strength. Limit the die bond pad surface temperature to 200°C maximum.

**Notes:**