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# PLL400-915AY

## 5V NARROWBAND PHASE-LOCKED LOOP

**Package: PLL400, 15.24mm x 15.24mm x 3mm**

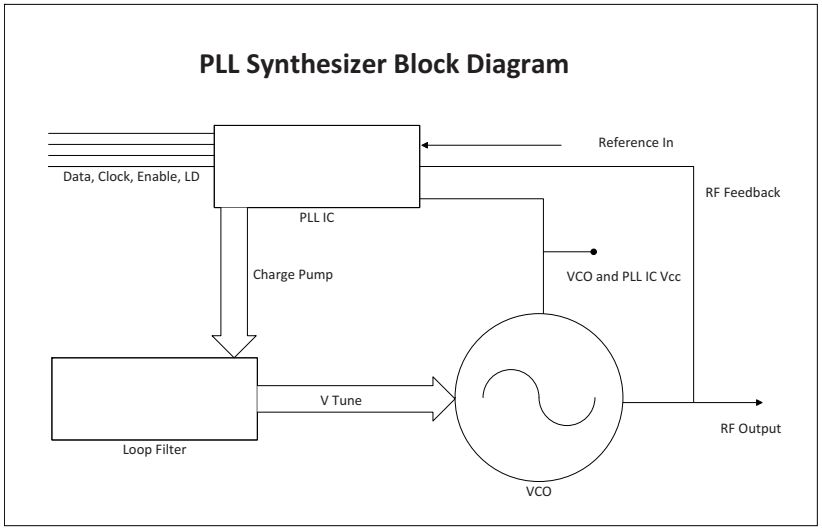
RoHS

## Features

- Low Phase Noise / Fast Settling Time
- SPI Bus Compatible
- Frequency: 902MHz to 928MHz
- Resonator: Aircoil
- PCB: FR4 and S1170
- Package Size: 15.24mm x 15.24mm x 3mm (0.6in x 0.6in x 0.118in)

## Applications

- Cellular Infrastructure
- RFID
- General Wireless




Functional Block Diagram

## Product Description

RFMD® offers complete Phase Locked Modules (PLLs) integrating a PLL IC, a VCO, loop filter components, and buffer amplifiers. RFMD has a broad selection of oscillator topologies, resonator technologies, supply voltages, and substrate materials available, allowing us to provide customers with a PLL solution that meets the specific cost, performance, and size requirements for their applications.

### Ordering Information

PLL400-915AY Contact us at 1-480-756-6070

### Optimum Technology Matching® Applied

| | | | |
|---|---|---|---|
| ☐ GaAs HBT | ☐ SiGe BiCMOS | ☐ GaAs pHEMT | ☐ GaN HEMT |
| ☐ GaAs MESFET | ☐ Si BiCMOS | ☐ Si CMOS | ☐ BiFET HBT |
| ☐ InGaP HBT | ☐ SiGe HBT | ☑ Si BJT | ☐ LDMOS |





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## Absolute Maximum Ratings

| Parameter | Rating | Unit |
|---|---|---|
| Operating Ambient Temperature | -40 to +85 | °C |
| Storage Temperature | -55 to +125 | °C |

**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.



RoHS (Restriction of Hazardous Substances): Compliant per EU Directive 2002/95/EC.

| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Overall** | | | | | |
| Frequency Range | 902 | 915 | 928 | MHz | |
| Step Size | | 200 | | kHz | |
| Settling Time | | 5 | 10 | ms | To within 1.0kHz |
| Output Power | 0 | 3 | 6 | dBm | |
| Output Phase Noise | | -87 | -81 | dBc/Hz | 1kHz |
| | | -111 | -105 | dBc/Hz | 10kHz |
| | | -133 | -127 | dBc/Hz | 100kHz |
| Spurious Product | | -80 | -70 | dBc | 200kHz |
| Reference Feedthrough | | -80 | -70 | dBc | |
| Harmonic Suppression | | -15 | -10 | dBc | 2nd harmonic |
| | | -20 | -10 | dBc | 3rd harmonic |
| Reference Oscillator Signal | | 10 | | MHz | Frequency |
| | 3 | | 5 | Vp-p | Amplitude |
| | | -145 | | dBc/Hz | Phase noise - 1kHz |
| | | 100 | | kΩ | Input impedance |
| Output Impedance | | 50 | | Ω | |
| **Power Supply** | | | | | |
| Operating Voltage | 4.75 | 5 | 5.25 | V | |
| Supply Current | | 22 | 30 | mA | |

## PLL Synthesizer Programming

Refer to Application Note 113, Option 20700.



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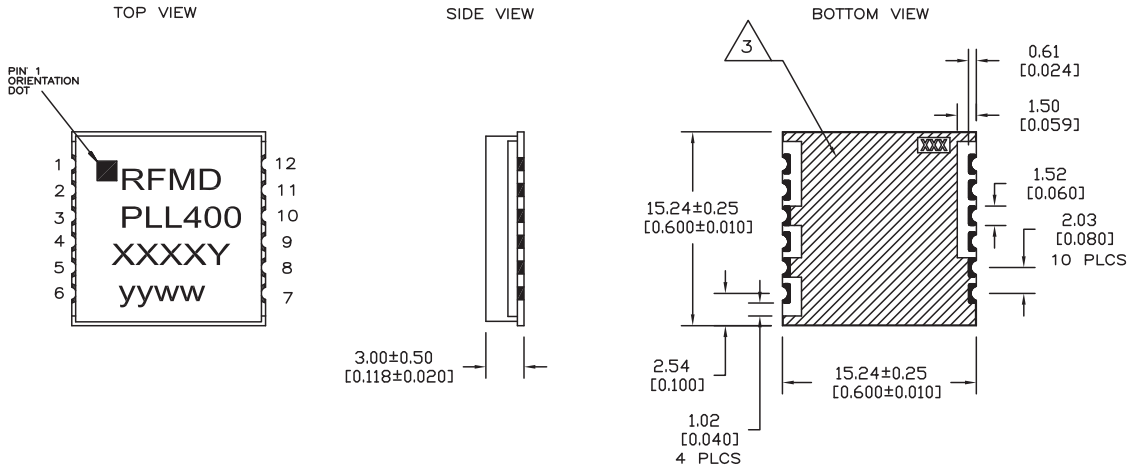
## Package Drawing & Pin Outs

15.24mm x 15.24mm x 3mm (0.6in x 0.6in x 0.118in)




| PIN OUT FOR PLL | |
|---|---|
| PIN | APPLICATION |
| 1 | CLOCK |
| 2 | DATA |
| 3 | ENABLE |
| 4 | REF. OSC IN |
| 6 | GROUND * |
| 7 | VCC (VCO) |
| 9 | RF OUT |
| 11 | LOCK DETECT |
| 12 | VCC (CHIP) |

ALL OTHER PINS ARE GROUND
* OPTIONAL MODULATION PORT

NOTE, UNLESS OTHERWISE SPECIFIED:

1. THE METAL CASE IS GROUND.
2. ALL HALF VIA CONTACTS ARE PLATED THRU FROM THE PAD ON THE TOP SIDE TO THE PAD ON THE BOTTOM SIDE OF THE BOARD.
3. HATCHED AREAS ARE GROUND AND ARE COVERED WITH LPI SOLDER MASK OVER BARE COPPER. ALL CONTACT AREAS ARE PLATED. SIGNAL VIAS MAY BE LOCATED WITHIN GROUND PLANE.
4. CROSS HATCHED AREA INDICATES AREA WHERE SOLDER MASK SHOULD BE APPLIED TO MOUNTING BOARD.
5. SUBSTRATE MATERIAL: FR-4.
6. XXXX REPRESENTS THE MODEL NUMBER.
7. yyww IS THE DATE CODE.
8. Y AT THE END OF MODEL NUMBER DESIGNATES RoHS COMPLIANCE.
9. DIMENSIONS ARE IN MILLIMETERS AND [INCHES].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