

Preliminary Technical Data
HMC1132
FEATURES

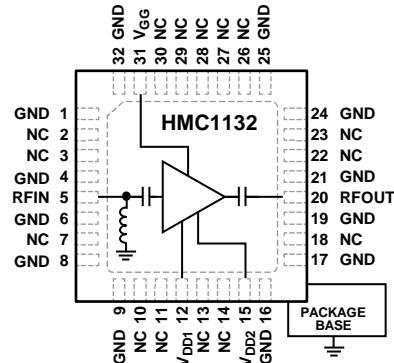
Saturated output power (P_{SAT}): 30.5 dBm at 22% power added efficiency (PAE)
High output IP3: 35 dBm
High gain: 22 dB
DC supply: 6 V at 600 mA
No external matching required
32-lead, 5 mm × 5 mm LFCSP package

APPLICATIONS

Point-to-point radios
Point-to-multipoint radios
VSAT and SATCOM
Military and space

GENERAL DESCRIPTION

The [HMC1132](#) is a four-stage, GaAs pHEMT MMIC, 1 watt power amplifier that operates between 27 GHz and 32 GHz. The [HMC1132](#) provides 22 dB of gain and 30.5 dBm of saturated output power at 22% PAE from a 6 V power supply. The [HMC1132](#) exhibits excellent linearity and it is optimized for high capacity, point-to-point and point-to-multipoint radio

FUNCTIONAL BLOCK DIAGRAM


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Figure 1.

systems. The amplifier configuration and high gain make it an excellent candidate for last stage signal amplification before the antenna.

The [HMC1132](#) amplifier input/outputs (I/Os) are internally matched to $50\ \Omega$. The device is supplied in a compact, leadless QFN, 5 mm × 5 mm surface-mount package.

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

$T_A = 25^\circ\text{C}$, $V_{DD} = V_{DD1} = V_{DD2} = 6 \text{ V}$, $I_{DD} = 600 \text{ mA}$.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		27		32	GHz	
GAIN Gain Variation over Temperature		20	22 0.036		dB dB/ $^\circ\text{C}$	
RETURN LOSS Input Output			6 14		dB dB	
POWER Output Power for 1 dB Compression Saturated Output Power	P _{1dB} P _{SAT}	28	30		dBm	
OUTPUT THIRD-ORDER INTERCEPT	IP3		35		dBm	Measurement taken at 6 V at 600 mA, $P_{OUT} \div \text{tone} = 20 \text{ dBm}$
TOTAL SUPPLY CURRENT	I _{DD}		600		mA	Adjust the amplifier gate control voltage (V_{GG}) between -2 V and 0 V to achieve an $I_{DD} = 600 \text{ mA}$, typical

TOTAL SUPPLY CURRENT BY V_{DD}

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT $V_{DD} = 5 \text{ V}$ $V_{DD} = 5.5 \text{ V}$ $V_{DD} = 6 \text{ V}$	I _{DD}		600		mA	Adjust the amplifier gate control voltage (V_{GG}) between -2 V and 0 V to achieve an $I_{DD} = 600 \text{ mA}$, typical
			600		mA	
			600		mA	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Drain Voltage Bias	7 V
RF Input Power (RFIN) ¹	18 dBm
Channel Temperature	150°C
Continuous P _{DISS} (T = 85°C) (Derate 61 mw/°C Above 85°C)	4.04 W
Thermal Resistance (R _{TH}) Junction to Ground Paddle	16.4°C/W
Maximum Peak Reflow Temperature	260°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
ESD Sensitivity (Human Body Model)	Class 1A, passed 250 V

¹ Maximum P_{IN} is limited to 18 dBm or thermal limits constrained by maximum power dissipation (see Figure 31), whichever is lower.

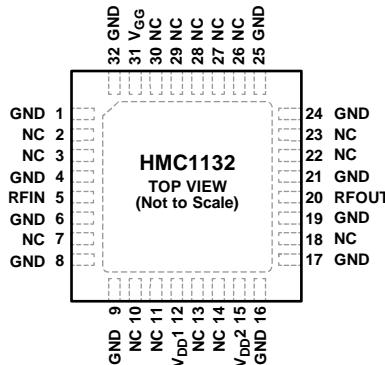
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. NC = NO CONNECT.
2. EXPOSED PAD. EXPOSED PAD MUST BE CONNECTED TO RF/DC GROUND.

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Figure 2. Pin Configuration

Table 4. Pad Function Descriptions

Pad No.	Mnemonic	Description
1, 4, 6, 8, 9, 16, 17, 19, 21, 24, 25, 32	GND	Ground. These pins are exposed ground paddles that must be connected to RF/dc ground.
2, 3, 7, 10, 11, 13, 14, 18, 22, 23, 26 to 30	NC	No Connect. These pins are not connected internally. However, all data was measured with these pins connected to RF/dc ground externally.
5	RFIN	RF Input. This pin is dc-coupled and matched to 50 Ω. See Figure 4 for the RFIN interface schematic.
12, 15	V _{DD1} , V _{DD2}	Drain Bias Voltage. External bypass capacitors of 100 pF, 10 nF, and 4.7 μF are required. See Figure 5 for the V _{DD1} and V _{DD2} interface schematic.
20	RFOUT	RF Output. This pin is ac-coupled and matched to 50 Ω. See Figure 6 for the RFOUT interface schematic.
31	V _{GG}	Gate Control for Amplifier. Adjust V _{GG} to achieve the recommended bias current. External bypass capacitors of 100 pF, 10 nF, and 4.7 μF are required. See Figure 7 for the V _{GG} interface schematic.
	EPAD	Exposed Paddle. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

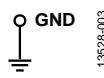


Figure 3. GND Interface

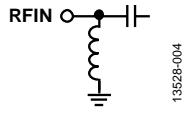


Figure 4. RFIN Interface

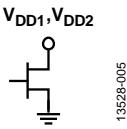
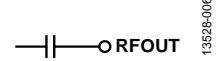
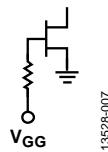
Figure 5. V_{DD1} and V_{DD2} Interface

Figure 6. RFOUT Interface

Figure 7. V_{GG} Interface

TYPICAL PERFORMANCE CHARACTERISTICS

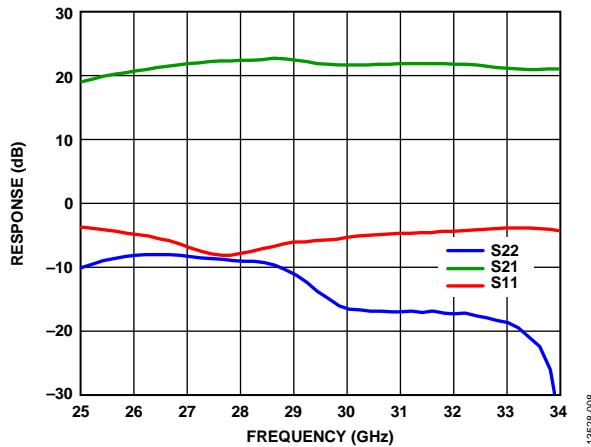


Figure 8. Broadband Gain and Return Loss vs. Frequency

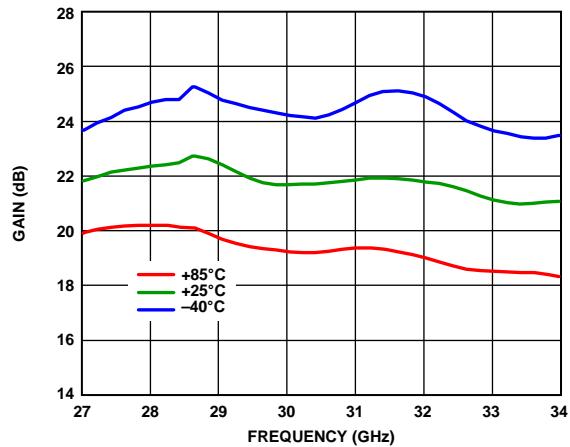


Figure 11. Gain vs. Frequency at Various Temperatures

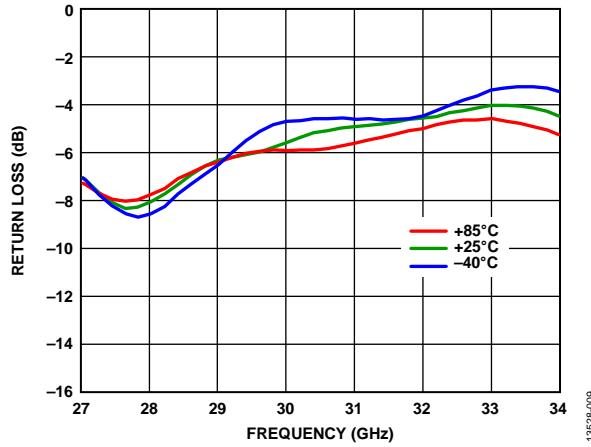


Figure 9. Input Return Loss vs. Frequency at Various Temperatures

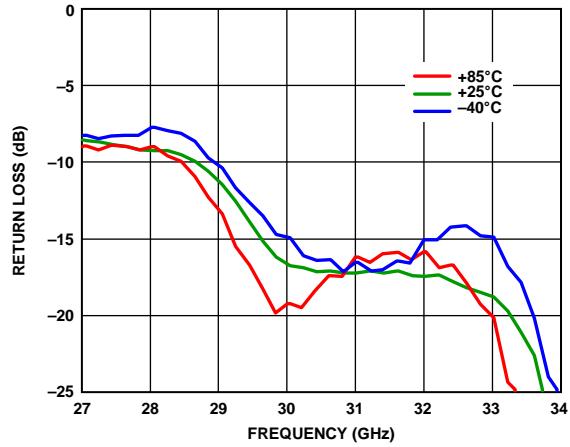


Figure 12. Output Return Loss vs. Frequency at Various Temperatures

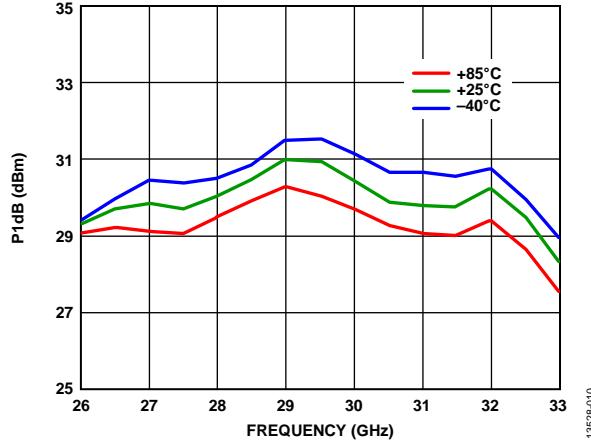


Figure 10. P1dB vs. Frequency at Various Temperatures

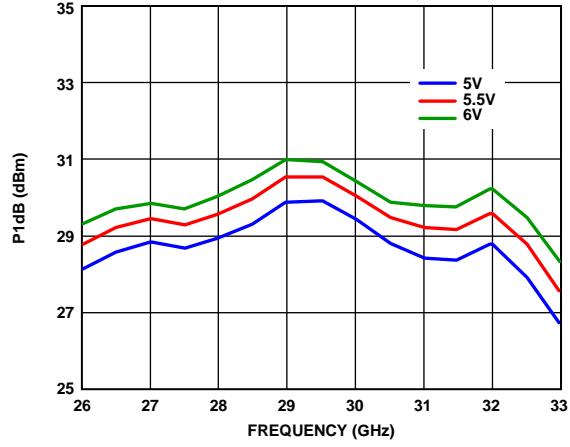
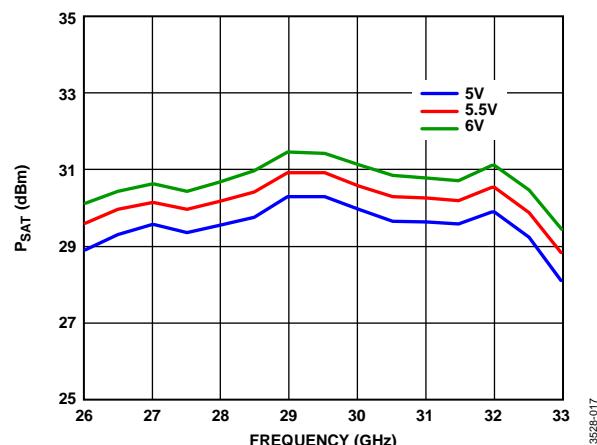
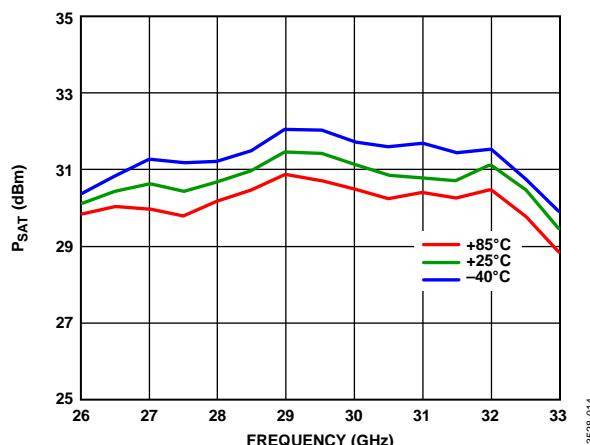
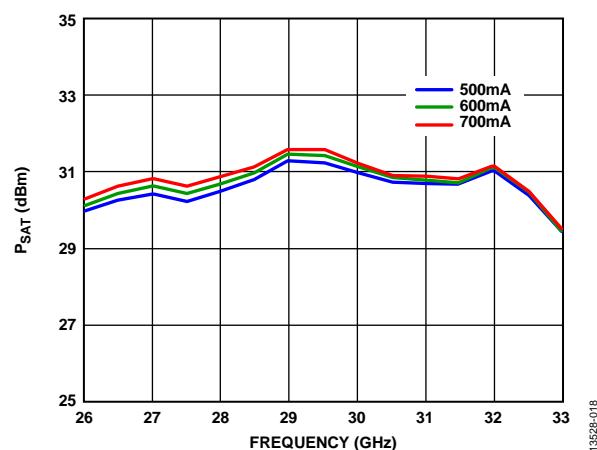
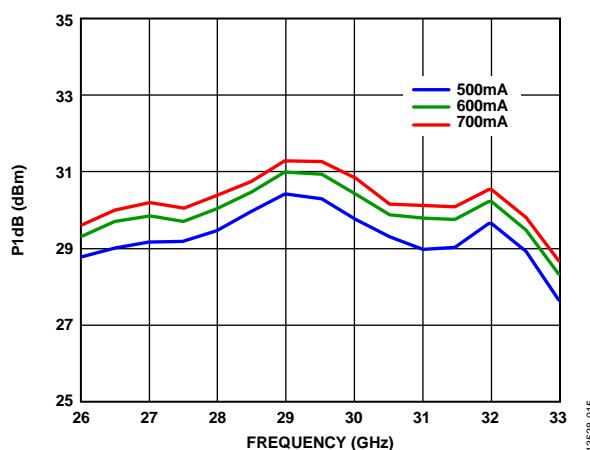


Figure 13. P1dB vs. Frequency at Various Supply Voltages



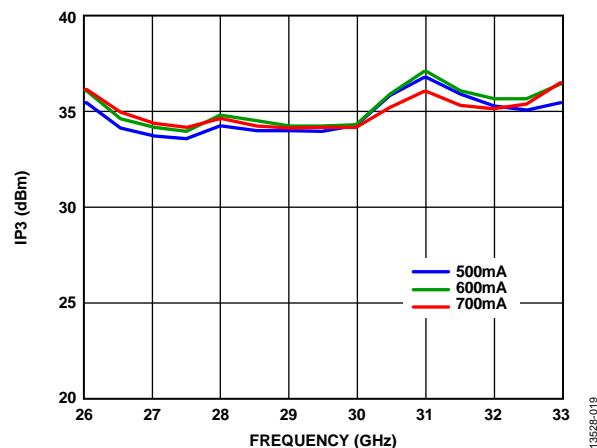
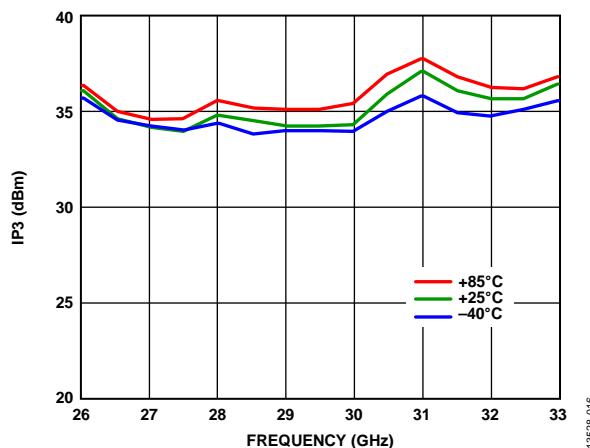
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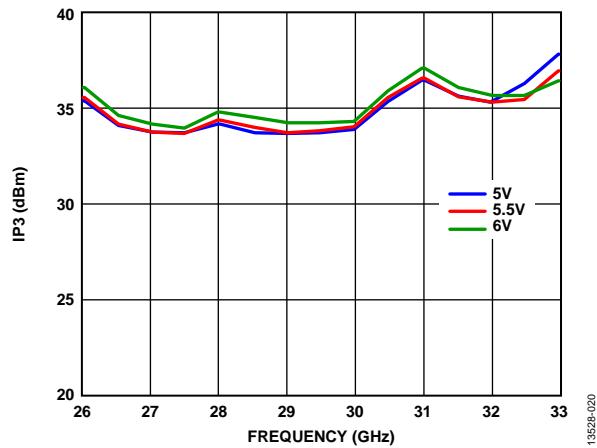
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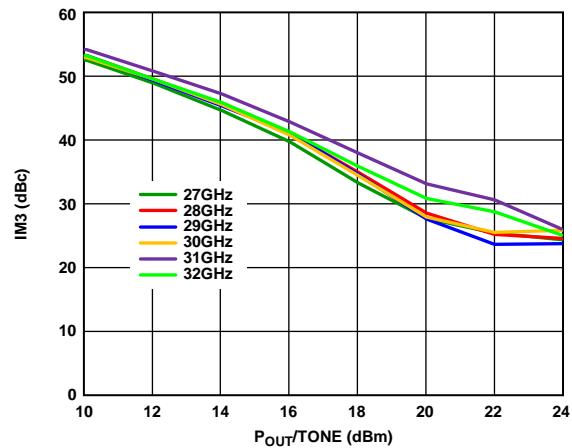


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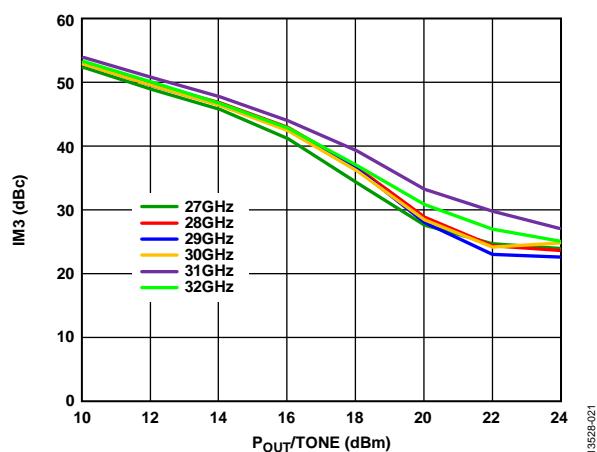
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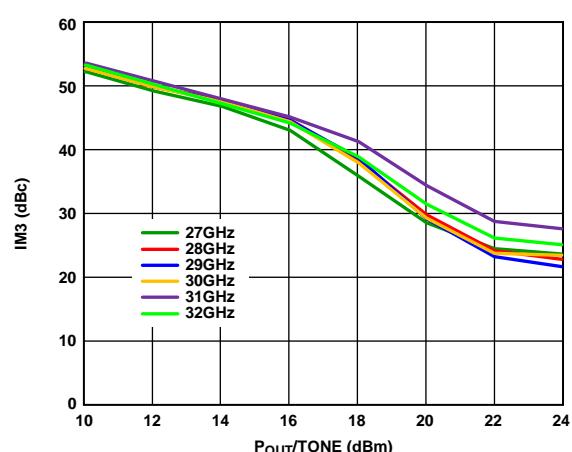
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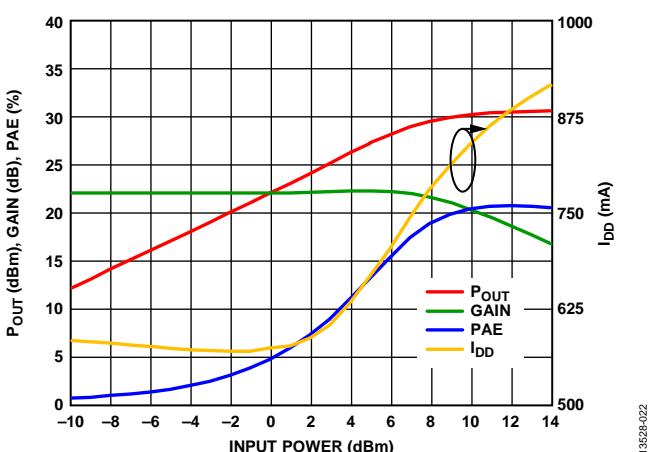
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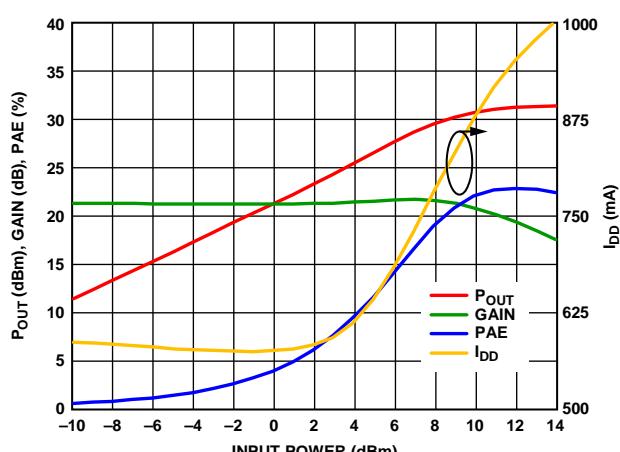
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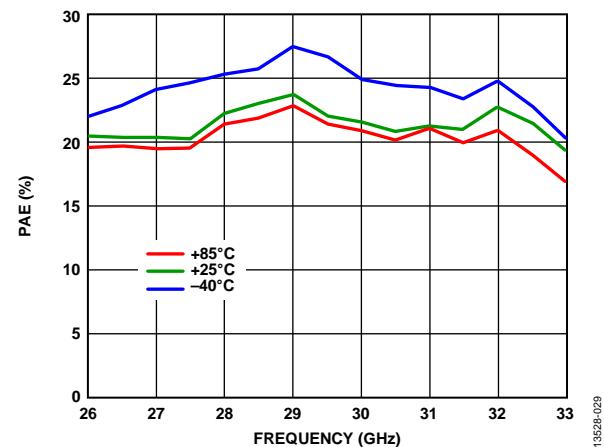
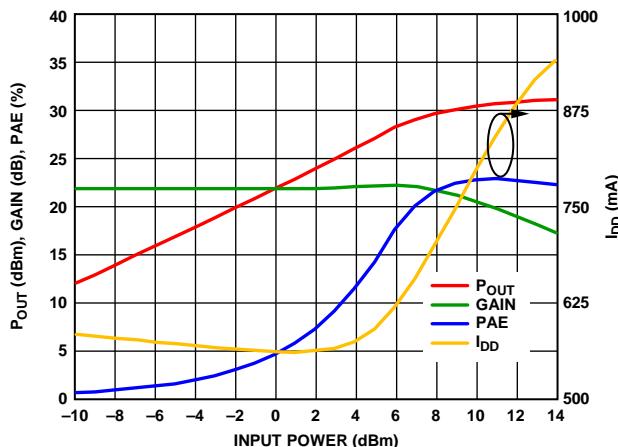
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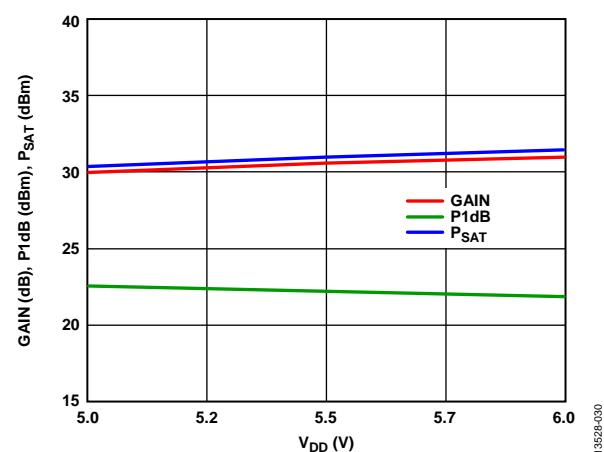
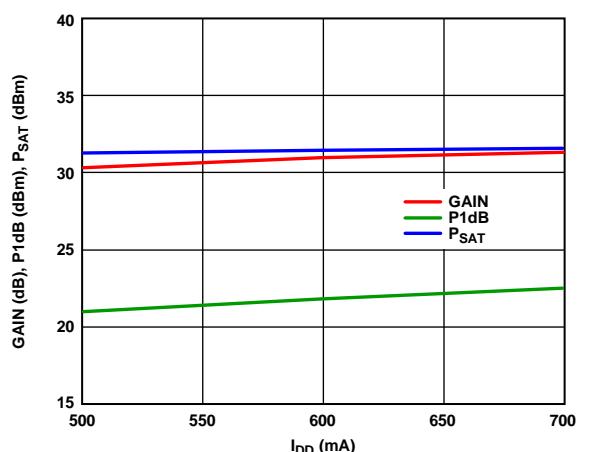


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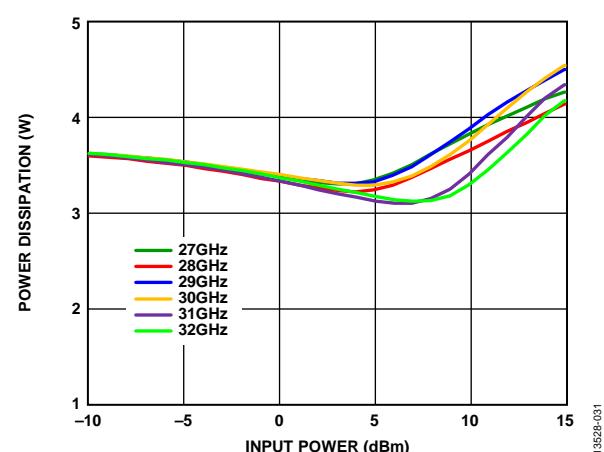
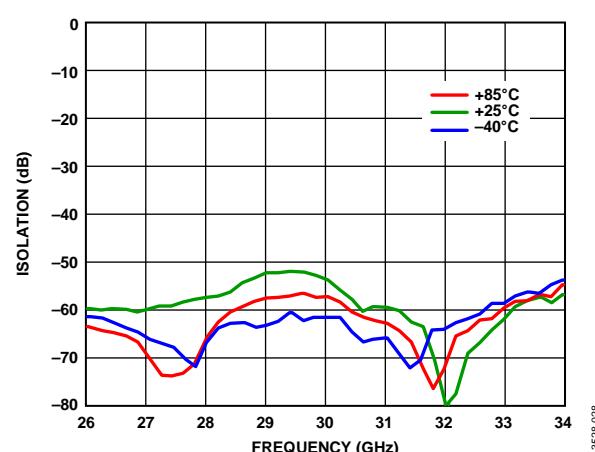
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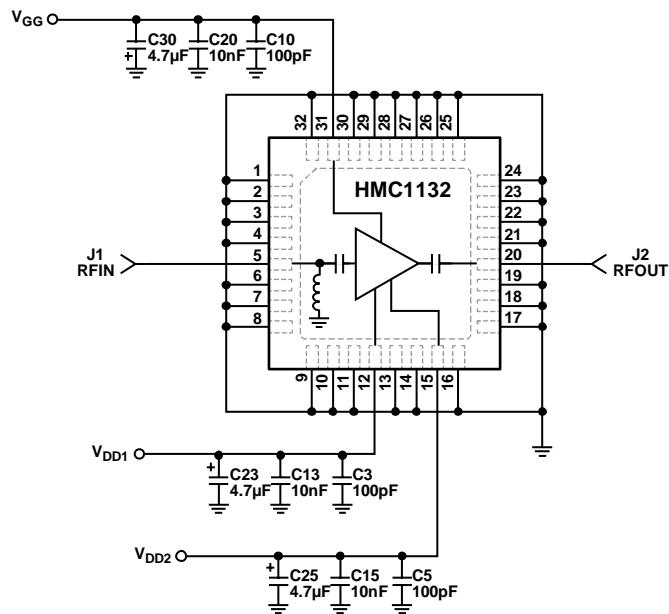


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APPLICATIONS INFORMATION

APPLICATION CIRCUIT



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Figure 32. Typical Application Circuit

EVALUATION PRINTED CIRCUIT BOARD (PCB)

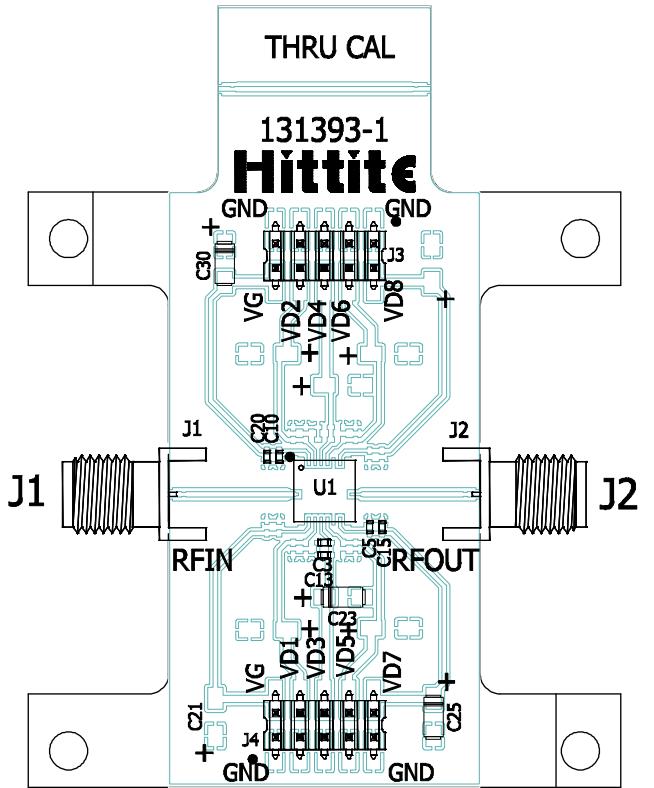


Figure 33. Evaluation Printed Circuit Board (PCB)

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BILL OF MATERIALS

Use RF circuit design techniques for the circuit board used in the application. Provide $50\ \Omega$ impedance to the signal lines and connect the package ground leads and exposed paddle directly to the ground plane, similar to that shown in Figure 33. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 33 is available from Analog Devices, Inc., upon request.

**Table 5. Bill of Materials for Evaluation PCB
EV1HMC1132LP5D**

Item	Description
J1, J2	Conn, SRI K connector.
J3, J4	DC pins.
C3, C5, C10	100 pF capacitors, 0402 package.
C13, C15, C20	10,000 pF capacitors, 0402 package.
C23, C25, C30	4.7 μ F capacitors, Case A package.
U1	HMC1132LP5DE amplifier.
PCB	131393 evaluation board. Circuit board material: Rogers 4350 or Arlon 25FR.

OUTLINE DIMENSIONS

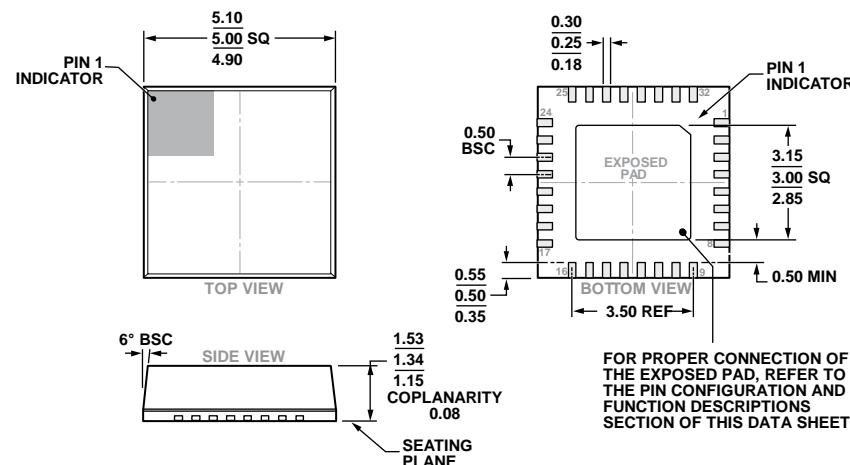


Figure 34. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 1.34 mm Package Height
(HCP-32-2)
Dimensions shown in millimeters

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