Digital Step Attenuator 50Ω DC-4000 MHz

15.5 dB, 0.5 dB Step
5 Bit, Serial Control Interface, Single Positive Supply Voltage, +3V

Product Features
- Single positive supply voltage, +3V
- Immune to latch up
- Excellent accuracy, 0.1 dB Typ
- Serial control interface
- Low Insertion Loss
- High IP3, +52 dBm typ
- Very low DC power consumption
- Excellent return loss, 20 dB Typ
- Small size 4.0 x 4.0 mm

DAT-15R5-SP+

CASE STYLE: DG983-1
PRICE: $3.55 ea. QTY. (20)

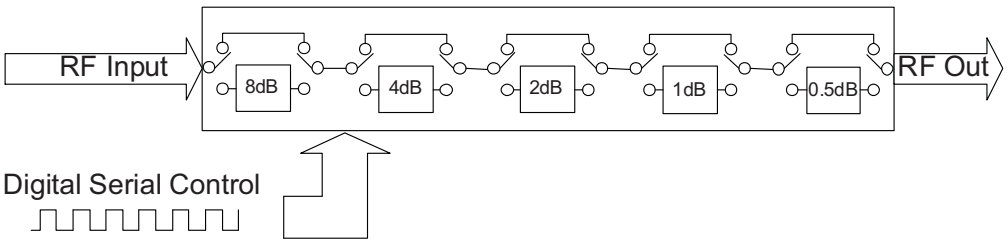
+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Not Recommended for New Designs
Recommended Replacement Part:
DAT-15R5A-SP+

Typical Applications
- Base Station Infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- Wireless Local Loop
- UNII & Hiper LAN
- Power amplifier distortion canceling loops

General Description
The DAT-15R5-SP+ is a 50Ω RF digital step attenuator that offers an attenuation range up to 15.5 dB in 0.5 dB steps. The control is a 5-bit serial interface, operating on a single +3 volt supply. The DAT-15R5-SP+ is produced using a unique CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic



RF Electrical Specifications, DC-4000 MHz, T_{AMB}=25°C, V_{DD}=+3V

Parameter	Freq. Range (GHz)	Min.	Typ.	Max.	Units
Accuracy @ **0.5 dB** Attenuation Setting	DC-1	G	0.03	0.1	-.
	1-2.2	G	0.05	0.15	-.
	2.2-4.0	G	0.1	0.3	-.
Accuracy @ **1 dB** Attenuation Setting	DC-1	G	0.02	0.1	-.
	1-2.2	G	0.05	0.15	-.
	2.2-4.0	G	0.1	0.3	-.
Accuracy @ **2 dB** Attenuation Setting	DC-1	G	0.05	0.15	-.
	1-2.2	G	0.15	0.25	-.
	2.2-4.0	G	0.2	0.45	-.
Accuracy @ **4 dB** Attenuation Setting	DC-1	G	0.07	0.2	-.
	1-2.2	G	0.15	0.25	-.
	2.2-4.0	G	0.18	0.45	-.
Accuracy @ **8 dB** Attenuation Setting	DC-1	G	0.03	0.2	-.
	1-2.2	G	0.15	0.25	-.
	2.2-4.0	G	0.5	0.8	-.
Insertion Loss (note 1) @ all attenuator set to 0 dB	DC-1	G	1.3	1.9	-.
	1-2.2	G	1.1	2.5	-.
	2.2-4.0	G	3.3	4.7	-.
Input IP3 (note 2) (at Min. and Max. Attenuation)	DC-2.2	G	+52	G	-.(
	2.2-4.0	G	+42	G	-.(
Input Power @ 0.2dB Compression (note 2) (at Min. and Max. Attenuation)	DC-4.0	G	+24	G	-.(
VSWR	DC-1	G	1.2	1.5	G
	1-2.2	G	1.2	1.5	G
	2.2-4.0	G	1.8	2.1	G

DC Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
V_{DD}, Supply Voltage	2.7		3.3	V
'$_{DD}$, Supply Current, quiescent (note 3)	G	G	100	µ
Control Input Low	G	G	0.3xV_{DD}	V
Control Input High	0.7xV_{DD}	G	G	V
Control Current	G	G	1	µ

Notes:
1. I. Loss values are de-embedded from test board Loss (test board's Insertion Loss: 0.10dB @100MHz, 0.35dB @1000MHz, 0.60dB @2200MHz, 0.75dB @4000MHz, 1.5dB @6000MHz).
2. Input IP3 and 1dB compression degrades below 1 MHz.
3. During turn-on and transition between attenuation states, device may draw up to 2mA.

Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	G	1.0	G	µSec
Switching Control Frequency	G	G	25	KHz

Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
V_{DD}	-0.3V Min., 4V Max.
Voltage on any input	-0.3V Min., V_{DD}+0.3V Max.
ESD, HBM	500V
ESD, MM	100V
Input Power	+24dBm

Permanent damage may occur if any of these limits are exceeded.

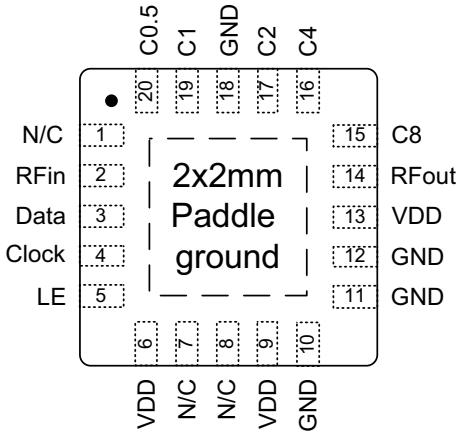
Pin Description

Function	Pin Number	Description
7M1	1	Not connected (Note 5)
RF in	2	RF in port (Note 1)
Data		Serial Interface data input (Note 3)
1~^)N	3	Serial Interface clock input
LE	5	Latch Enable Input (Note 2)
V_{DD}	6	Power Supply
7M1	H	Not connected
7M1	8	Not connected
V_{DD}	A	Power Supply
GND	10	Ground connection
GND	11	Ground connection
GND	12	Ground connection (Note 7)
V_{DD}	13	Power Supply
RF out	14	RF out port (Note 1)
C8	15	Control for attenuation bit, 8 dB (Note 4)
13	16	Control for attenuation bit, 4 dB (Note 4)
C2	17	Control for attenuation bit, 2 dB (Note 4)
GND	18	Ground Connection
C1	19	Control for attenuation bit, 1 dB (Note 4)
C0.5	20	Control for attenuation bit, 0.5 dB (Note 4)
GND	Paddle	Paddle ground (Note 6)

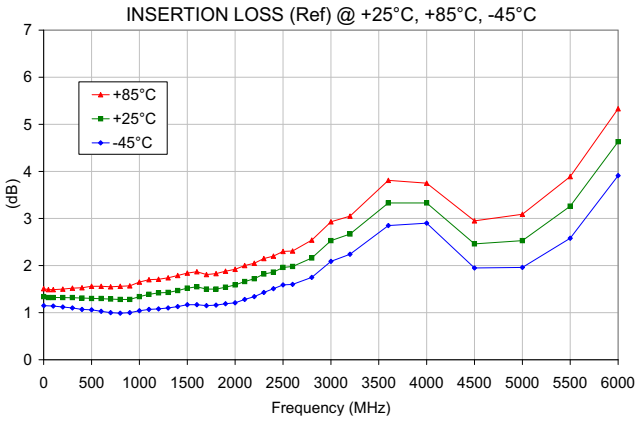
7^"~!@

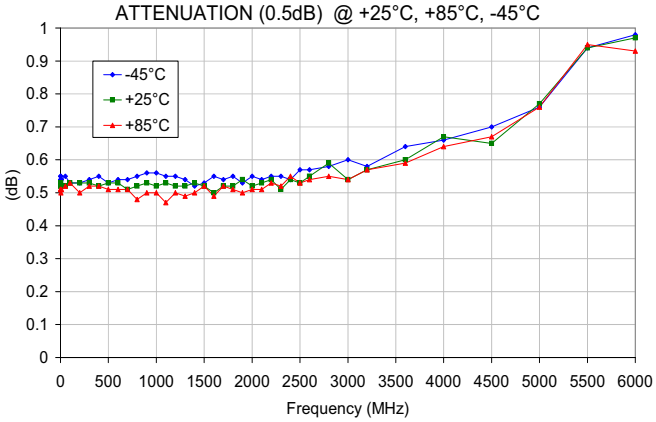
1. Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
2. Latch Enable (LE) has an internal 100KΩ resistor to V_{DD}.
3. Place a 10KΩ resistor in series, as close to pin as possible to avoid freq. resonance.
4. Refer to Power-up Control Settings.
5. Place a shunt 10KΩ resistor to GND.
6. The exposed solder pad on the bottom of the pachkage (see Pin configuration) must be grounded for proper device operation.
7. Ground must be less than 80 mil (0.08") from Pin 12 for proper device operation.

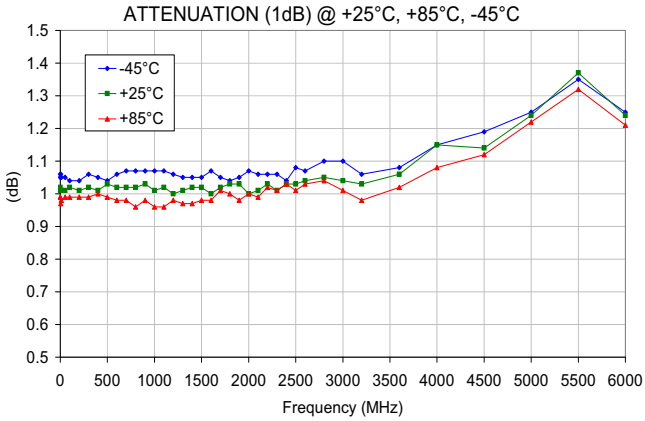
Pin Configuration (Top View)

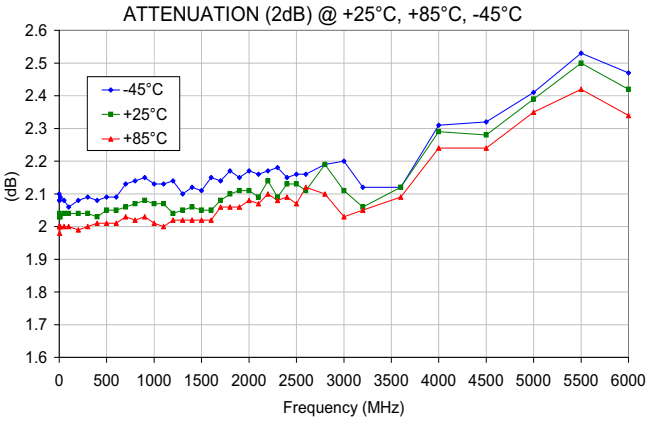


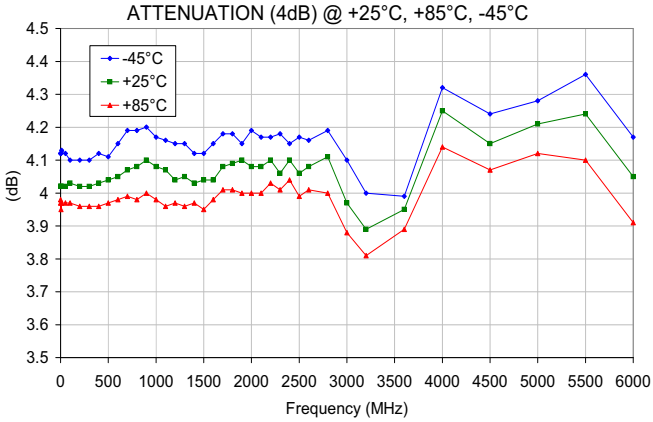
Typical Performance Curves

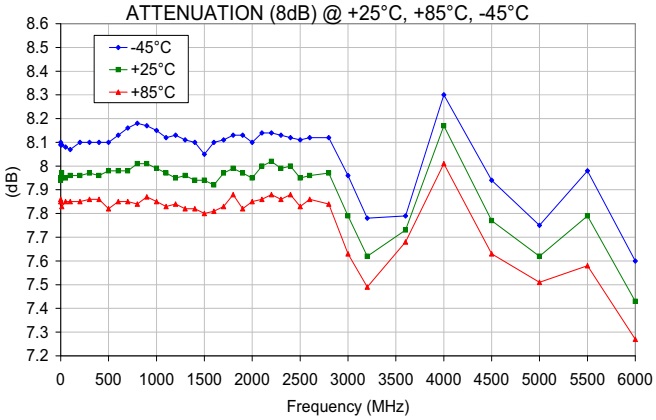




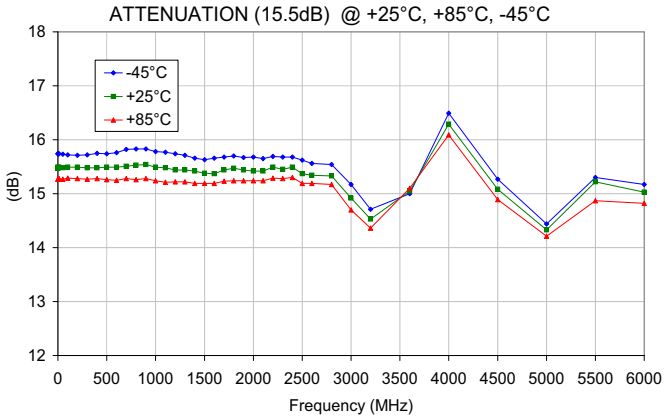


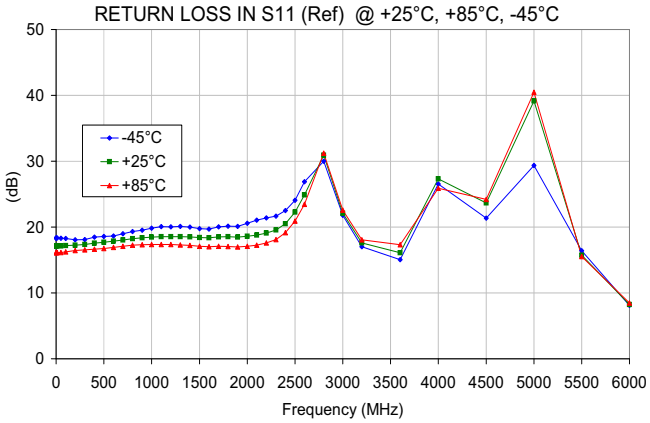


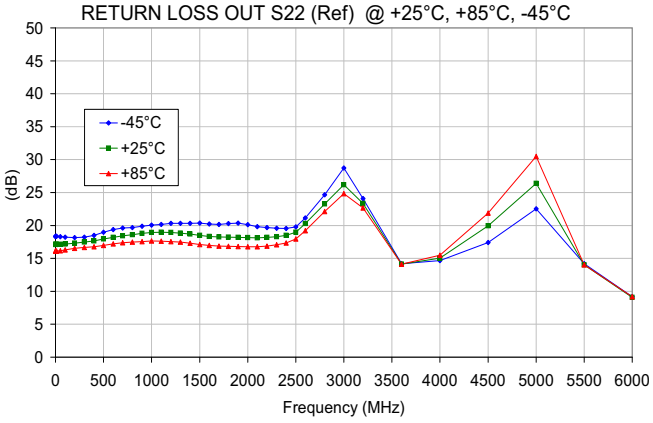


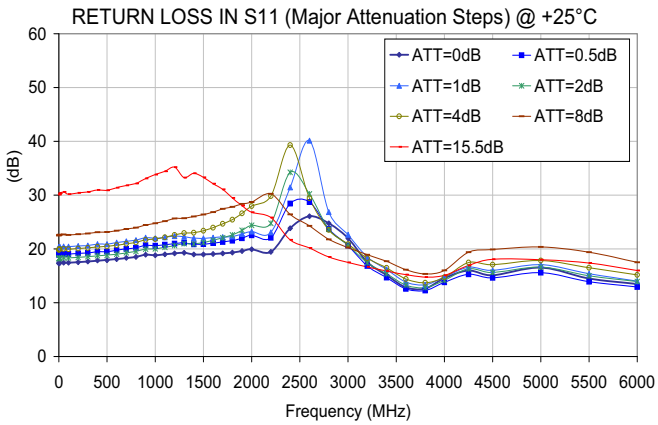


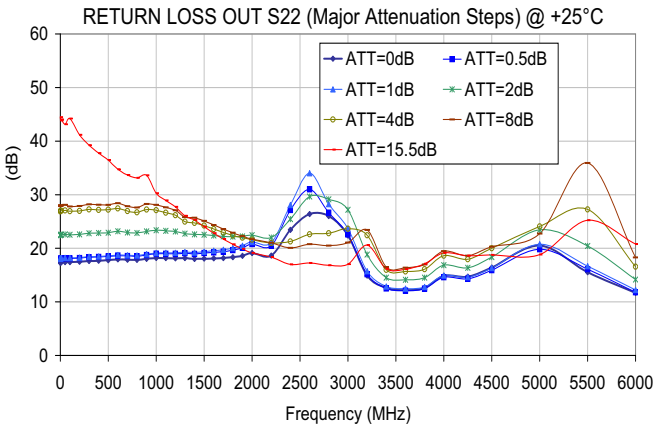
Typical Performance Curves



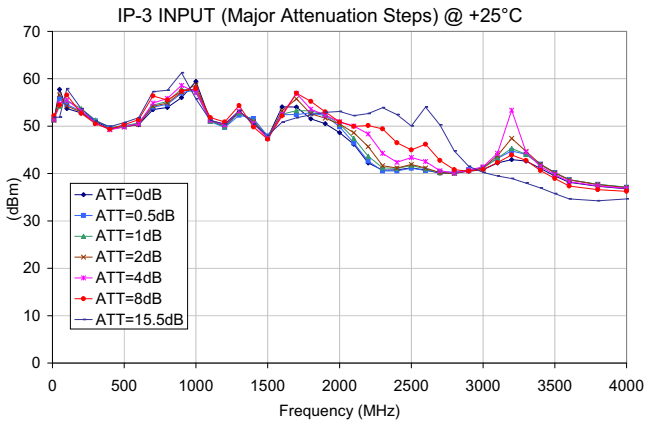


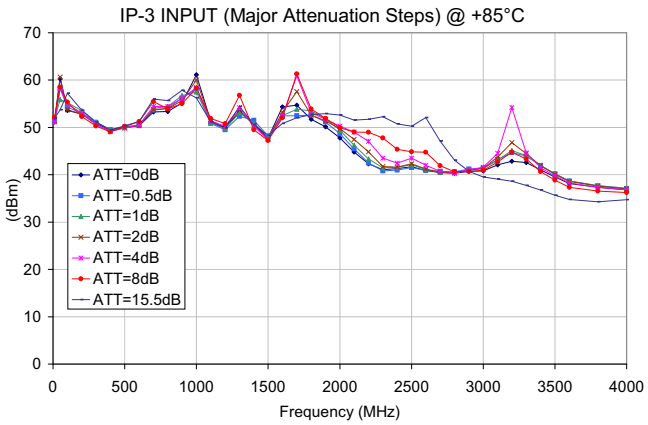


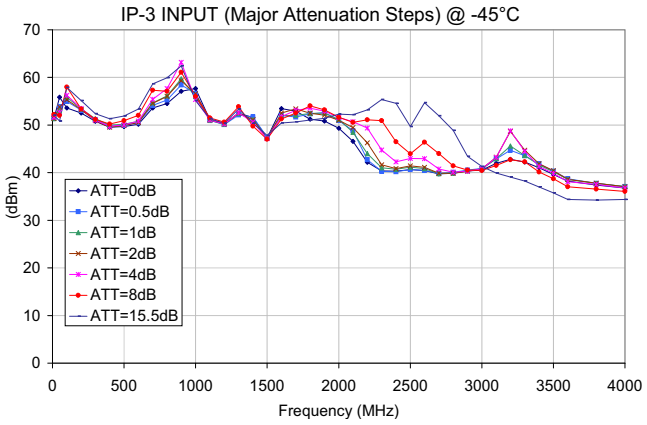


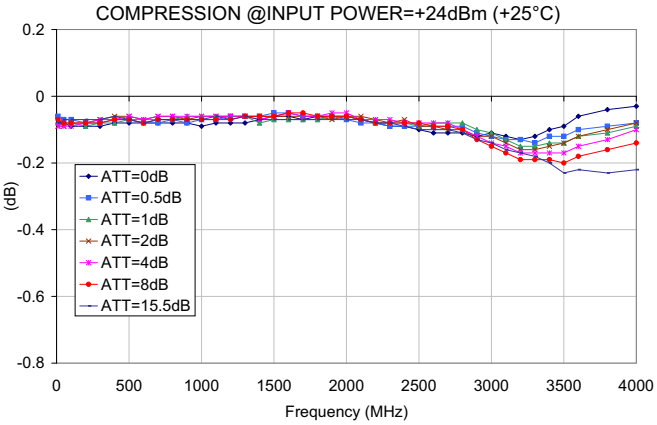


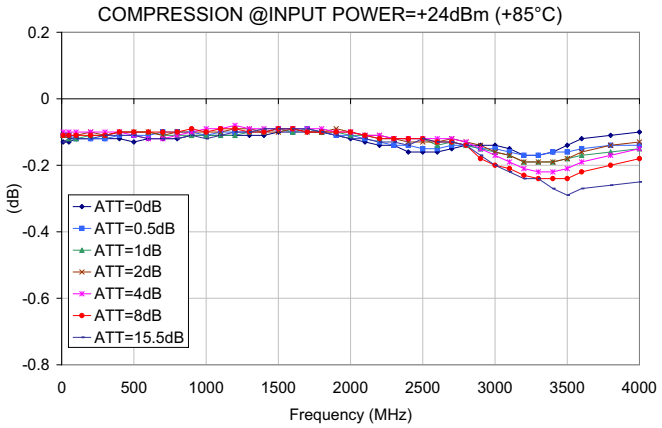
Typical Performance Curves

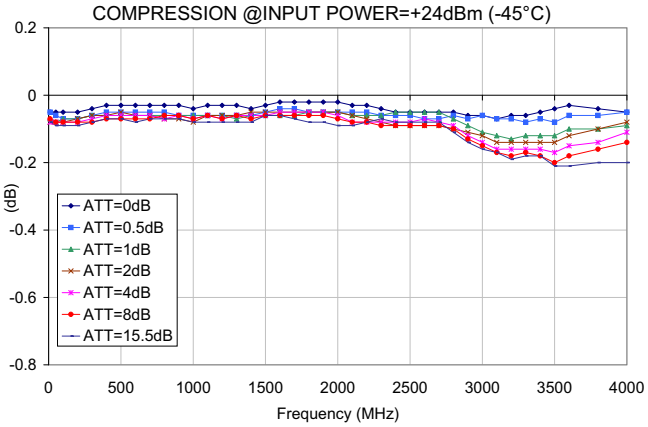




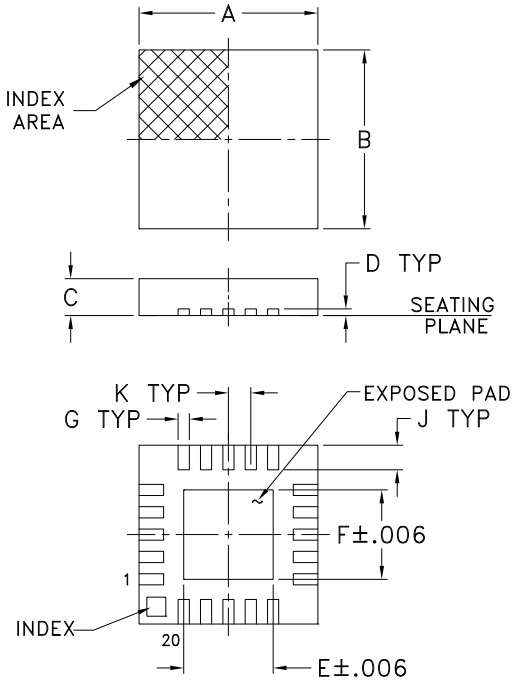




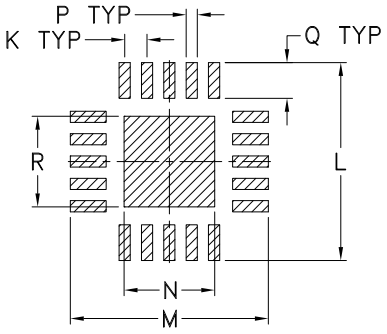




Outline Drawing (DG983-1)

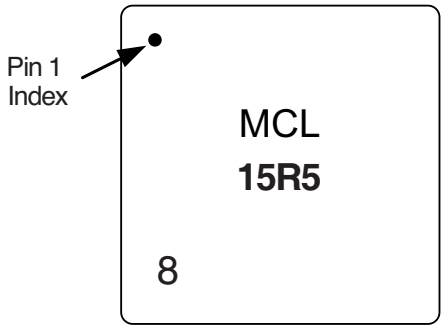


PCB Land Pattern



Suggested Layout,
Tolerance to be within ±.002

Device Marking

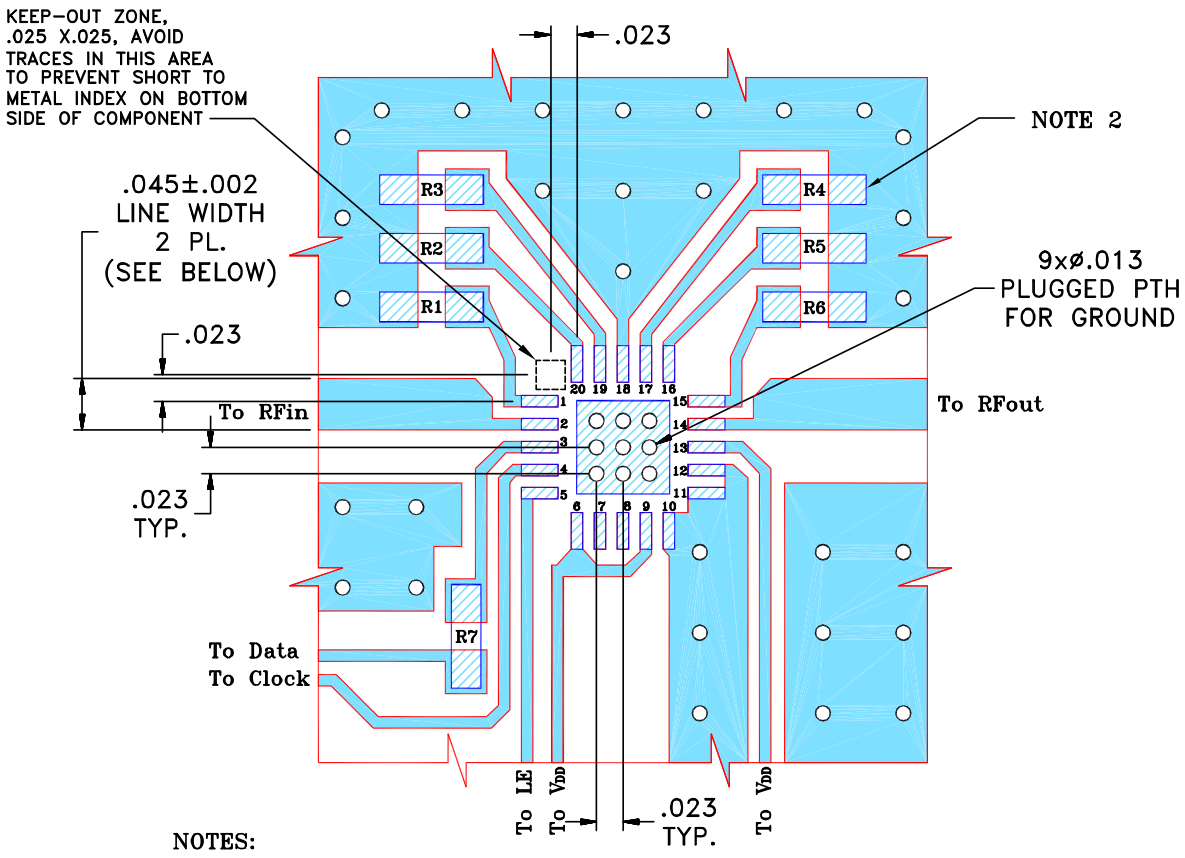


Outline Dimensions (inch)

A	B	C	D	E	F	G	H	J	K	˘	ˇ	ˆ	P	˙	˝	WT. GRAMS
.157	**.157**	**.035**	**.008**	**.081**	**.081**	**.010**	**—**	**.022**	**.020**	**.177**	**.177**	**.081**	**.010**	**.032**	**.081**	˜!"
"˜!!	"˜!!	!˜#!	0.20	2.06	2.06	0.25	%	0.56	!˜$!	"˜$!	"˜$!	2.06	0.25	!˜&	2.06	

Suggested Layout for PCB Design (PL-199)

The suggested Layout shows only the footprint area of the DAT, and the components located near this area (i.e.: R1-R7). For the complete Layout, see photo and schematic diagram on page 11 of 12.



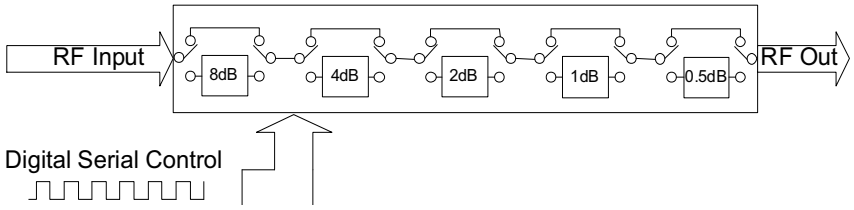
NOTES:

1. TRACE WIDTH IS SHOWN FOR FR4 WITH DIELECTRIC THICKNESS .025"±.002". COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. 0603 SIZE CHIP FOOT PRINTS SHOWN FOR REFERENCE, VALUES OF RESISTORS WILL VARY BASED ON APPLICATION.
3. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

DENOTES PCB COPPER LAYOUT WITH SMOBC (SOLDER MASK OVER BARE COPPER)

DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

Simplified Schematic



The DAT-15R5-SP+ Serial interface consists of 5 control bits that select the desired attenuation state, as shown in Table 1: Truth Table

Table 1. Truth Table

Attenuation State	C8	C4	C2	C1	C0.5
Reference	!	!	!	!	!
0.5 (dB)	!	!	!	!	
1 (dB)	!	!	!		!
2 (dB)	!	!		!	!
4 (dB)	!		!	!	!
8 (dB)		!	!	!	!
15.5 (dB)					

Note: Not all 32 possible combinations of C0.5 - C8 are shown in table

The serial interface is a 5-bit serial in, parallel-out shift register buffered by a transparent latch.

It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by **Figure 1** :Serial Interface Timing Diagram) and **Table 2** :Serial Interface AC Characteristics).

Figure 1: Serial Interface Timing Diagram

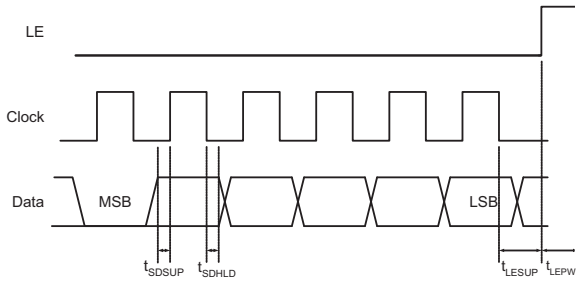


Table 2. Serial Interface AC Characteristics

Symbol	Parameter	Min.	Max.	Units
$f_{0-?}$	Serial data clock frequency (Note 1)		!	MHz
)clkH	Serial clock HIGH time	B!		/(
)ClkL	Serial clock LOW time	B!		/(
)LESUP	LE set-up time after last clock falling edge	!		/(
)LEPW	LE minimum pulse 23*)4	B!		/(
)SDSUP	Serial data set-up time before clock rising edge	!		/(
)SDHLD	Serial data hold time after clock falling edge	!		/(

Note 1. fclk verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10MHz to verify fclk specification.

The DAT-15R5-SP+, uses a common 5-bit serial word format, as shown in **Table 3**: 5-Bit attenuator Serial Programming Register Map.

The second bit B4 corresponds to the 8-dB Step and the last bit B0 corresponds to the 0.5 dB step.

Table 3. 5-Bit attenuator Serial Programming Register Map

B5	B4	B3	B2	B1	B0
!	C&	C"	C2	C	C0.5

MSB (first in)

LSB (last in)

Note: The start bit (B5) must always be low to prevent the attenuator from entering an unknown state.

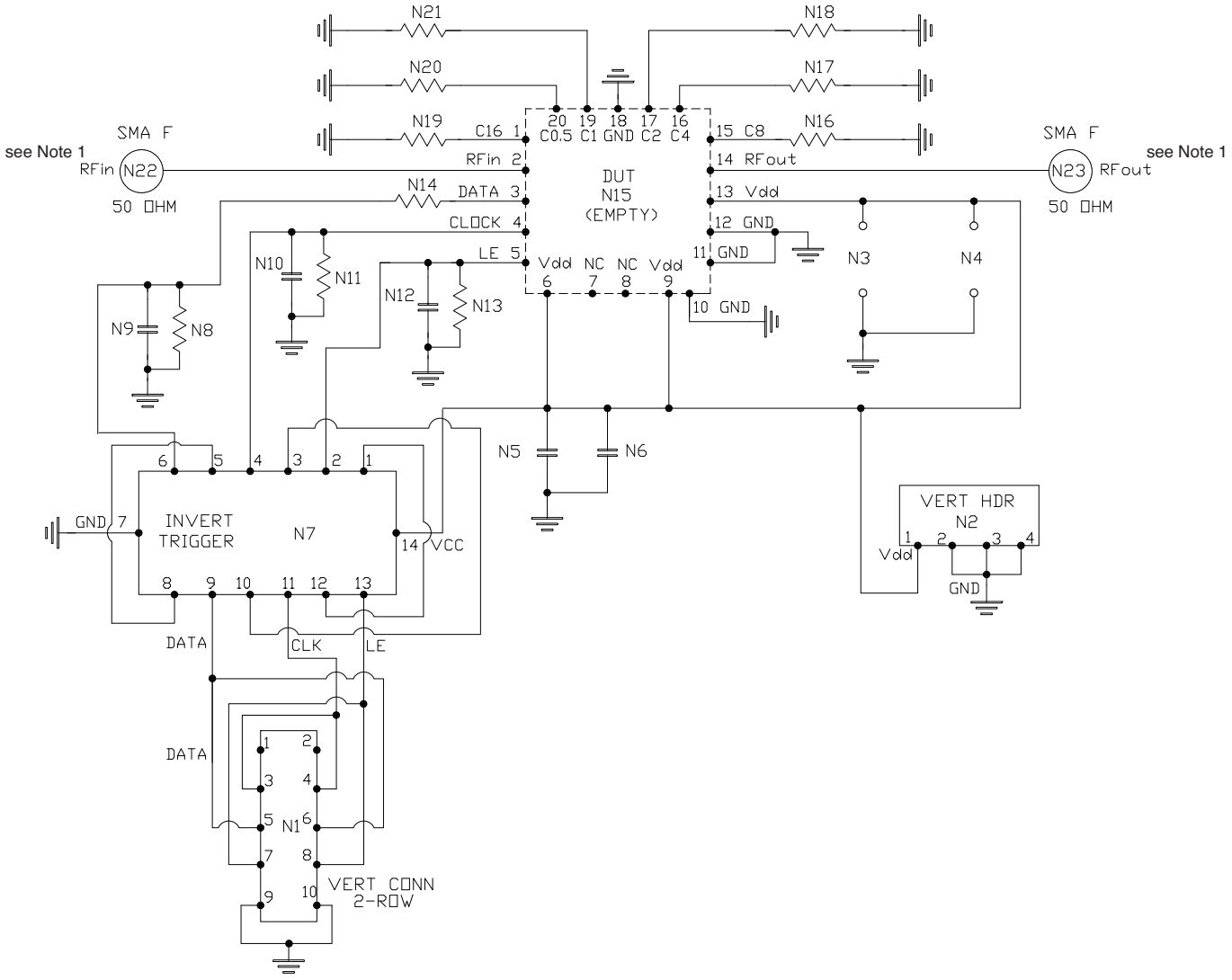
Power-up Control Settings

The DAT-15R5-SP+ always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial serial control word is provided.

When the attenuator powers up, the five control bits are set to whatever data is present on the five data inputs (C0.5 to C8).

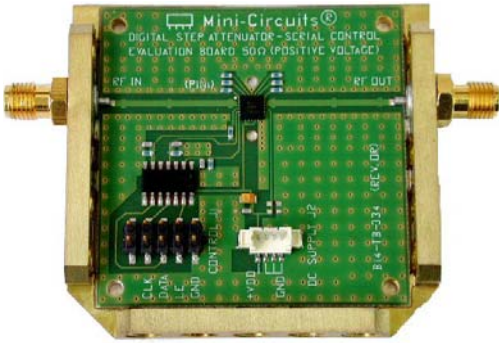
This allows any one of the 32 attenuation settings to be specified as the power-up state.

TB-334 Evaluation Board Schematic Diagram



Note 1: Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.

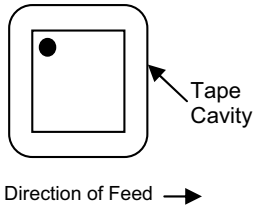
Bill of Materials	
N8, N11, N13, N14, N16-N21	Resistor 0603 10 KOhm +/- 1%
N5, N9, N10 & N12	NPO Capacitor 0603 100pF +/- 5%
N6	Tantalum Capacitor 0805 100nF +/- 10%
N7	Hex Invert Schmitt Trigger MSL1



TB-334

Tape and Reel Packaging Information

Table T&R

TR No.	No. of Devices	Reel Size	Tape Width	Pitch	Unit Orientation
F87	Small quantity standards 20, 50, 100, 200	7 inch	12 mm	8 mm	
	3000 (Standard)	13 inch			