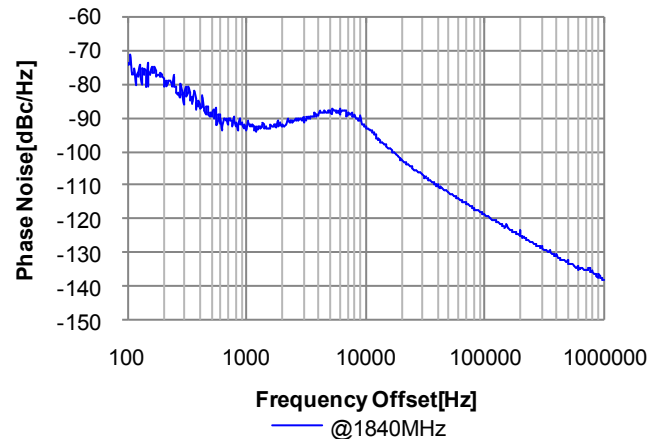


Features

- 3 wire serial Fractional PLL
- Sub-Compact Size 0.6"x0.6"x0.15"
- Low phase noise (typ. -88@1kHz)
- Programming : ADF4156(ADI)

Applications

- SATCOM radio link
- Receiver
- Test Equipment
- Radar
- Point-to-Point radio
- MMDS
- WiMAX

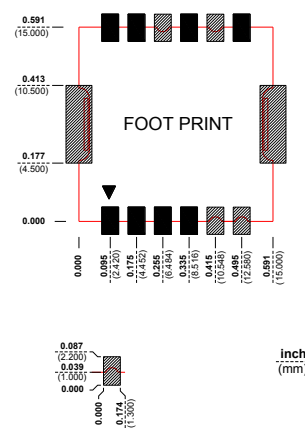
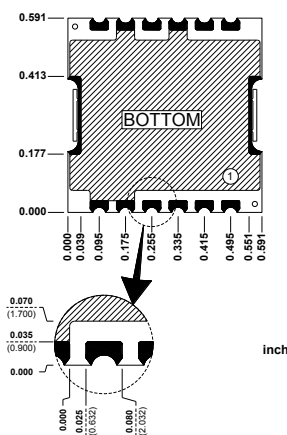
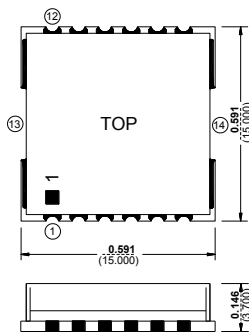


Electrical Characteristics



Parameter	Units	Min	Typ	Max
Operating Frequency Range	MHz	1800		1880
Step Size	kHz		100	
Settling Time	msec		0.88	
Output Power	dBm	+1.0	+3.0	+5.0
Output Impedance	Ω		50	
Phase Noise	@1kHz offset	dBc/Hz	-88	-83
	@10kHz offset	dBc/Hz	-92	-87
	@100kHz offset	dBc/Hz	-118	-113
	@1MHz offset	dBc/Hz	-138	-133
2nd Harmonic Suppression	dBc		-25	-20
Sideband Spurious Suppression	dBc			-65
Reference	Input Frequency	MHz	10	250
	Input Level	dBm	-5	+5
VCO Power Supply (Vcc)	Voltage	Vdc	5.0	
	Current	mA	40	50
PLL Power Supply (Vcp)	Voltage	Vdc	5.0	
	Current	mA	10	15
Operating Temp. Range	$^{\circ}\text{C}$	-40		+85

Dimensions



PIN CONNECTIONS	
1	CLK
2	DATA
3	LE
4	Ref. In
5-6	GND
7	Vcc(VCO)
8	GND
9	RF Out
10	GND
11	Lock Detect
12	Vcp(PLL)
13-14	GND

PACKAGE DRAWING : PS12-L

■ Programming Setting - ADF4156(ADI)

Analog Devices Evaluation Software

File Settings Help

RF Powerdown Disabled
 CSR Enabled
 LDP = 3
 Lowest Spur Mode
 Lowest Noise Mode

RF Section
 RF VCO Output Frequency: 1840.00000MHz
 PFD Frequency: 26000.00000kHz
 REF IN Frequency: 26.00000MHz
 Modulus: 260
 Channel Step Size: 100.00000kHz
 RF Prescaler: 4/5

RF Section
 RF Charge Pump Current Setting: 0.3125 mA
 RF PD Polarity Positive
 RF Counter Reset Disabled
 CP 3 State Off

Muxout
 Digital Lock Detect

Phase
 Phase value: 1
 Clock Divider mode: Disabled
 Clock Divider value: 0 Enter

ADF4156

Currently Loaded in Registers:

MSB	Binary	LSB	Hex
00000000000000000000000000000000	100	4	
001100000011000110000011001000000			30230640
00000000000000000000000000000001			9
00010000000000000001000100000100010			10008822
			01000011 43

All RF Registers Updated
 R0 Updated
 R1 Updated
 R2 Updated
 R3 Updated
 R4 Updated

Spurious Optimisation Sweep
 Frequency Sweep
 Frequency Hop

RF Output Frequency

Synthesizer Frequency

Enter the Reference Frequency (MHz): 26.000000

PLL

Enter the Channel Step Resolution (kHz): 100.000000

VCO

Enter the RF Output Frequency (MHz): 1840.000000

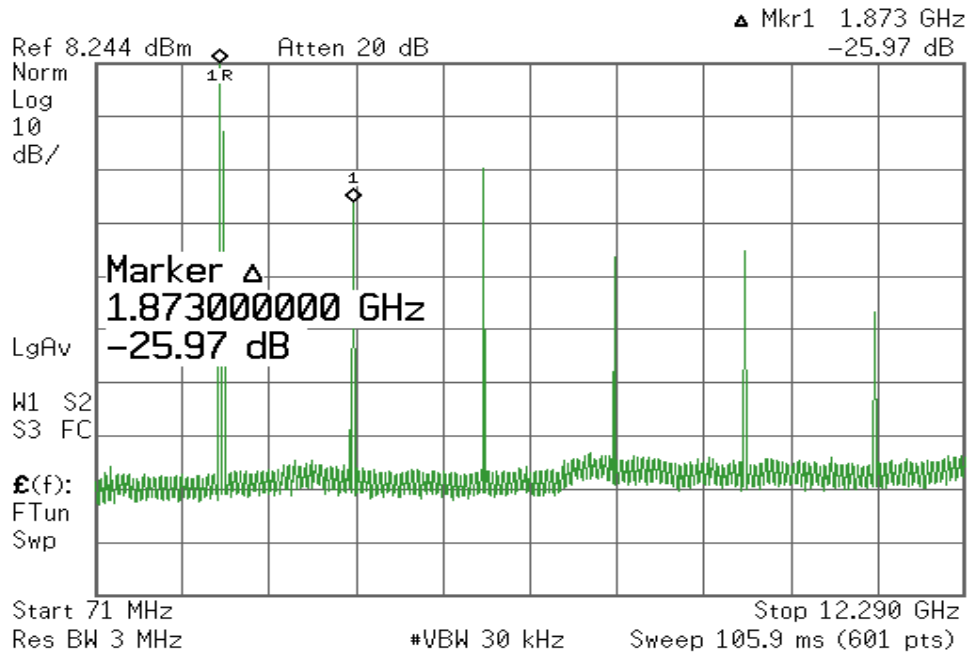
Legend:
 Changing Allowed (White)
 Not Changeable (Blue)

INT: 70 MOD: 260 FRAC: 200 P: 4 R: 1
 PFD Freq = Reference Freq * Doubler / R INT = RF Freq / PFD Freq

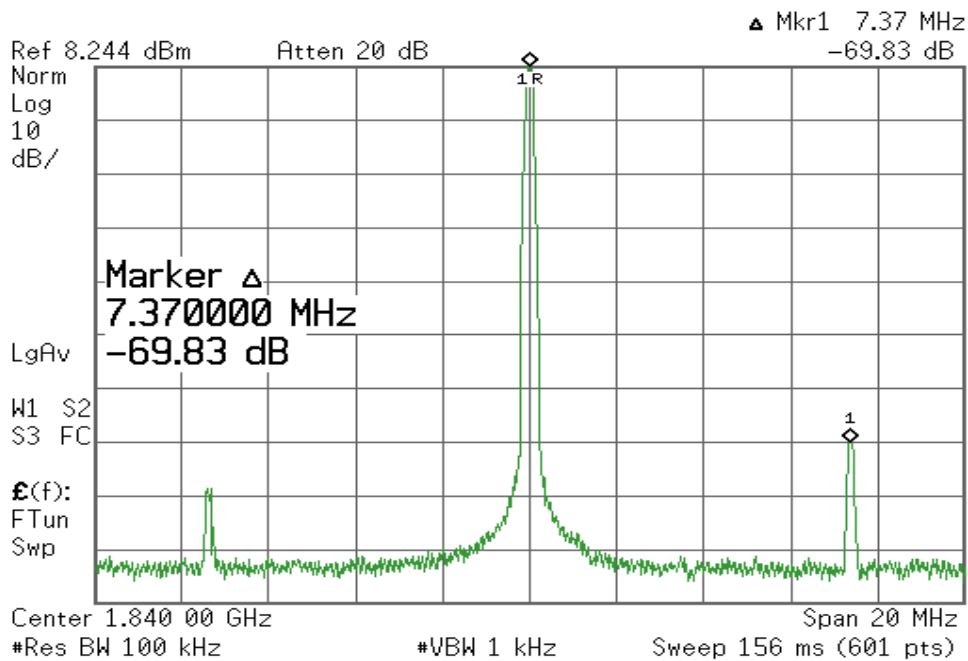
Increment by one channel step (Normal Mode). Update R0.
 Decrement by one channel step (Normal Mode). Update R0.
 Update R0 and R1 (Normal Mode)
 Exit Window
 Update R0 and R1 (LCD Mode)
 Increment by one channel step (LCD Mode). Update R0 and R1.
 Decrement by one channel step (LCD Mode). Update R0 and R1.

LCD Mode: This will automatically calculate the lowest common denominator, and use this as the fraction numerator and denominator.
 Normal Mode: This will use the default modulus as the denominator.
 Example: If the fraction = 40/100. The LCD Mode will program the fraction as 2/5. The Normal Mode will program the fraction as 40/100

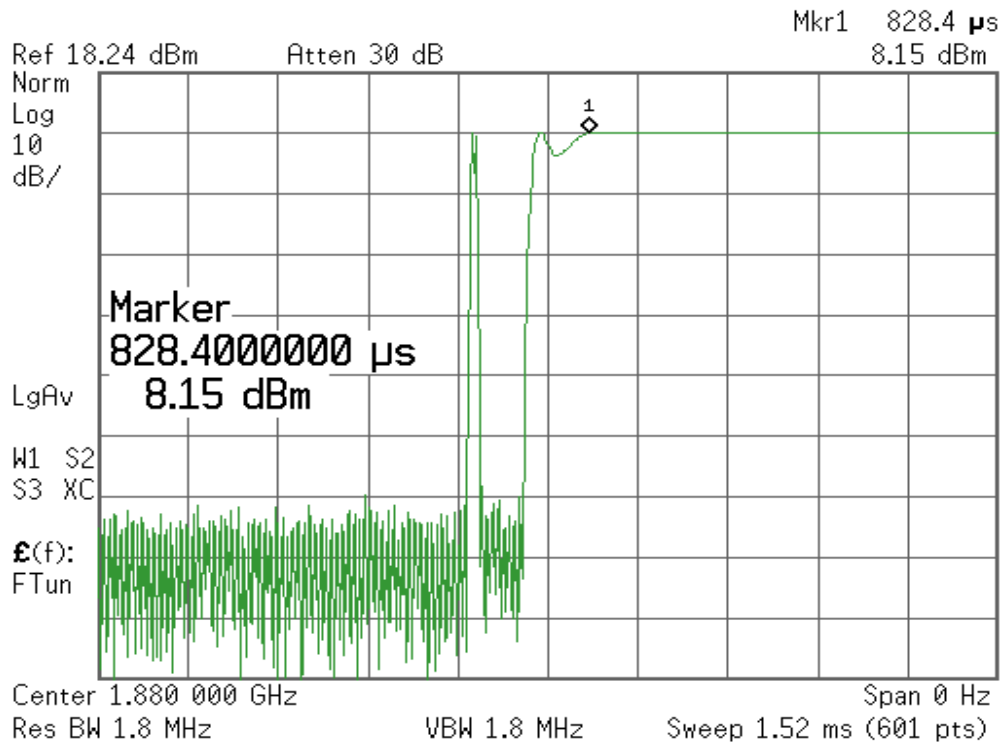
Harmonic Suppression



Sideband Spurious Suppression



Lock Time (1800MHz→1880MHz)



Lock Time (1880MHz→1800MHz)

