Digital Step Attenuator 50Ω DC-4000 MHz

15.5 dB, 0.5 dB Step
5 Bit, Parallel Control Interface, Single Positive Supply Voltage, +3V

Product Features
- Single positive supply voltage, +3V
- Immune to latch up
- Excellent accuracy, 0.1 dB Typ
- Parallel control interface
- Low Insertion Loss
- High IP3, +52 dBm typ
- Very low DC power consumption
- Excellent return loss, 20 dB Typ
- Small size 4.0 x 4.0 mm

DAT-15R5-PP+

CASE STYLE: DG983-1
PRICE: $3.55 ea. QTY. (20)

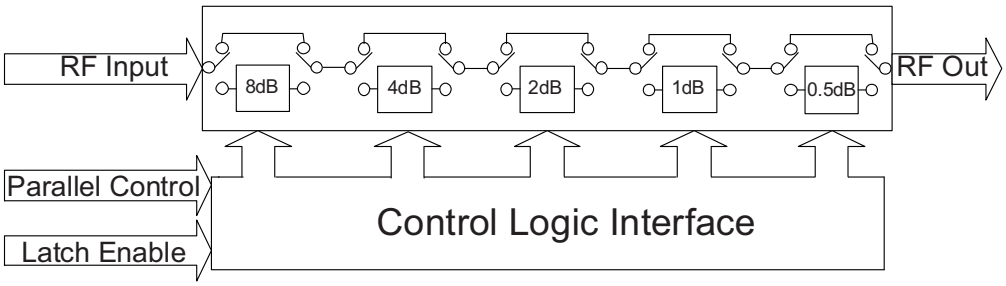
+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Not Recommended for New Designs
Recommended Replacement Part:
DAT-15R5A-PP+

Typical Applications
- Base Station Infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- Wireless Local Loop
- UNII & Hiper LAN
- Power amplifier distortion canceling loops

General Description
The DAT-15R5-PP+ is a 50Ω RF digital step attenuator that offers an attenuation range up to 15.5 dB in 0.5 dB steps. The control is a 5-bit parallel interface, operating on a single +3 volt supply. The DAT-15R5-PP+ is produced using a unique CMOS process on silicon, offering the performance of GaAs, with the advantages of conventional CMOS devices.

Simplified Schematic



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RF Electrical Specifications, DC-4000 MHz, T_{AMB}=25°C, V_{DD}=+3V

Parameter	Freq. Range (GHz)	Min.	Typ.	Max.	Units
Accuracy @ **0.5 dB** Attenuation Setting	DC-1	G	0.03	0.1	-.
	1-2.2	G	0.05	0.15	-.
	2.2-4.0	G	0.1	0.3	-.
Accuracy @ **1 dB** Attenuation Setting	DC-1	G	0.02	0.1	-.
	1-2.2	G	0.05	0.15	-.
	2.2-4.0	G	0.1	0.3	-.
Accuracy @ **2 dB** Attenuation Setting	DC-1	G	0.05	0.15	-.
	1-2.2	G	0.15	0.25	-.
	2.2-4.0	G	0.2	0.45	-.
Accuracy @ **4 dB** Attenuation Setting	DC-1	G	0.07	0.2	-.
	1-2.2	G	0.15	0.25	-.
	2.2-4.0	G	0.18	0.45	-.
Accuracy @ **8 dB** Attenuation Setting	DC-1	G	0.03	0.2	-.
	1-2.2	G	0.15	0.25	-.
	2.2-4.0	G	0.5	0.8	-.
Insertion Loss (note 1) @ all attenuator set to 0dB	DC-1	G	1.3	1.9	-.
	1-2.2	G	1.1	2.5	-.
	2.2-4.0	G	3.3	4.7	-.
Input IP3 (note 2) (at Min. and Max. Attenuation)	DC-2.2	G	+52	G	-.(
	2.2-4.0	G	+42	G	-.(
Input Power @ 0.2dB Compression (note 2) (at Min. and Max. Attenuation)	DC-4.0	G	+24	G	-.(
VSWR	DC-1	G	1.2	1.5	G
	1-2.2	G	1.2	1.5	G
	2.2-4.0	G	1.8	2.1	G

DC Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
V_{DD}, Supply Voltage	2.7		3.3	V
$'_{DD}$, Supply Current, quiescent (note 3)	G	G	100	µ
Control Input Low	G	G	0.3xV_{DD}	V
Control Input High	0.7xV_{DD}	G	G	V
Control Current	G	G	1	µ

Notes:
1. I. Loss values are de-embedded from test board Loss (test board's Insertion Loss: 0.10dB @100MHz, 0.35dB @1000MHz, 0.60dB @2200MHz, 0.75dB @4000MHz, 1.5dB @6000MHz).
2. Input IP3 and 1dB compression degrades below 1 MHz.
3. During turn-on and transition between attenuation states, device may draw up to 2mA.

Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	G	1.0	G	µ˜)
Switching Control Frequency	G	G	25	KHz

Absolute Maximum Ratings

Parameter	Ratings
Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
V_{DD}	-0.3V Min., 4V Max.
Voltage on any input	-0.3V Min., V_{DD}+0.3V Max.
ESD, HBM	500V
ESD, MM	100V
Input Power	+24dBm

Permanent damage may occur if any of these limits are exceeded.

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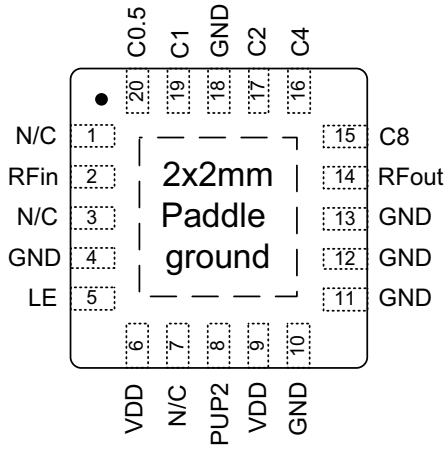
Pin Description

Function	Pin Number	Description
7M1	1	Not connected (Note 3)
RF in	2	RF in port (Note 1)
7M1		Not connected (Note 3)
GND	3	Ground connection
LE	5	Latch Enable Input (Note 2)
V_{DD}	6	Power Supply
7M1	H	Not connected
PUP2	8	Power up selection bit
V_{DD}	A	Power Supply
GND	10	Ground connection
GND	11	Ground connection
GND	12	Ground connection (Note 5)
GND	13	Ground connection
RF out	14	RF out port (Note 1)
C8	15	Control for attenuation bit, 8 dB
13	16	Control for attenuation bit, 4 dB
C2	17	Control for attenuation bit, 2 dB
GND	18	Ground Connection
C1	19	Control for attenuation bit, 1 dB
C0.5	20	Control for attenuation bit, 0.5 dB
GND	Paddle	Paddle ground (Note 4)

Pin Configuration (Top View)



7˜"˜!@

1. Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.
2. Latch Enable (LE) has an internal 100KΩ resistor to V_{DD}.
3. Place a 10KΩ resistor to GND.
4. The exposed solder pad on the bottom of the package (See Pin Configuration) must be grounded for proper device operation.
5. Ground must be less than 80 mil (0.08") from Pin 12 for proper device operation.

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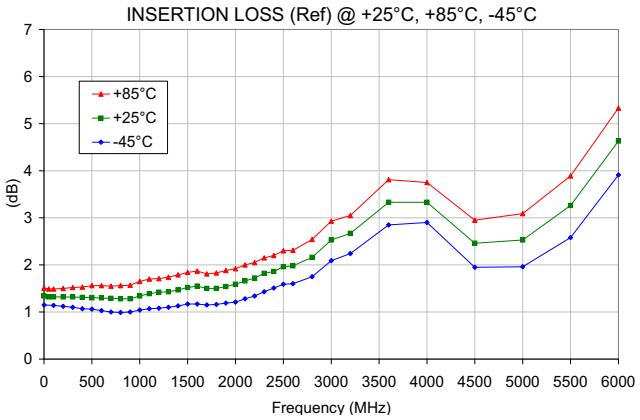
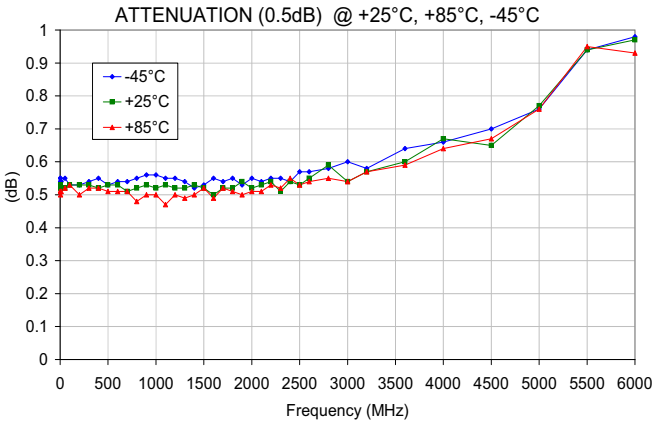
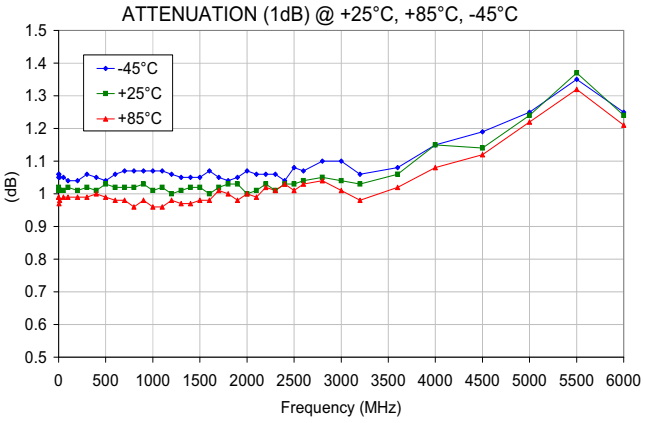
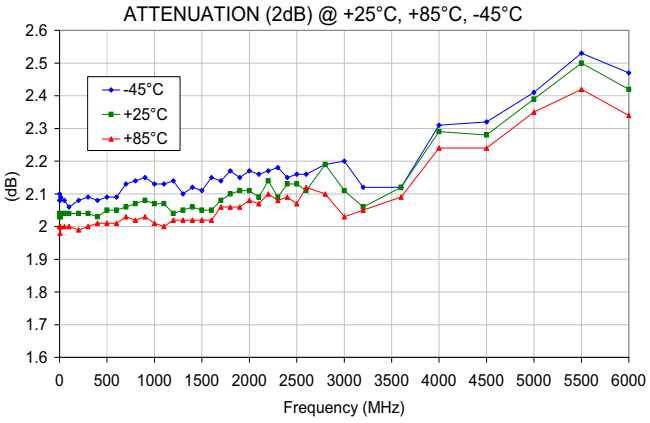
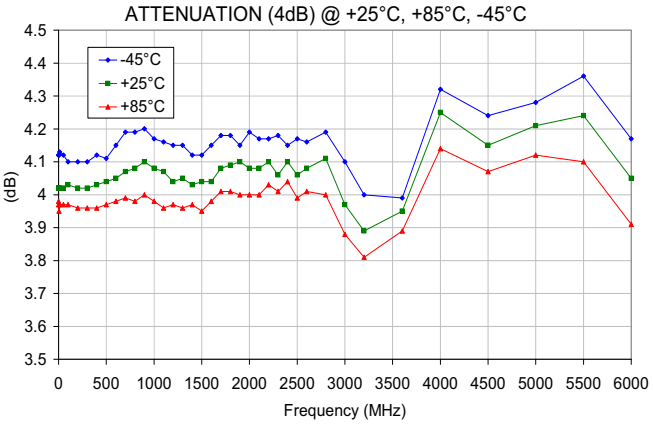
Typical Performance Curves

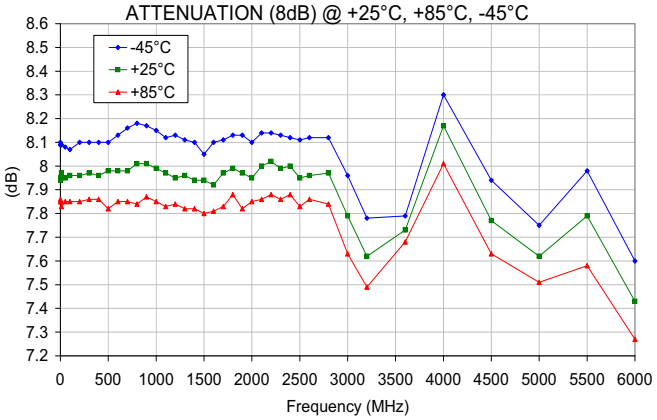












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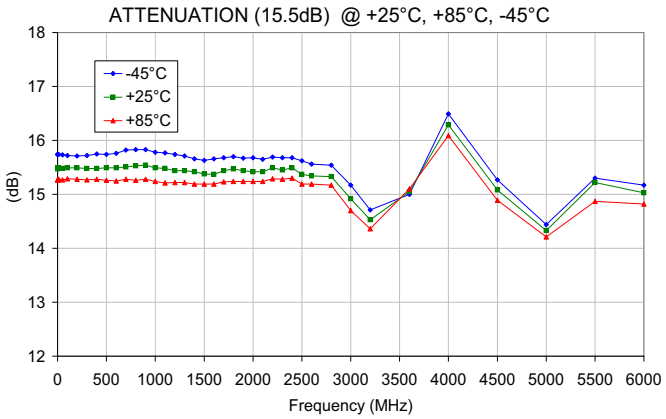
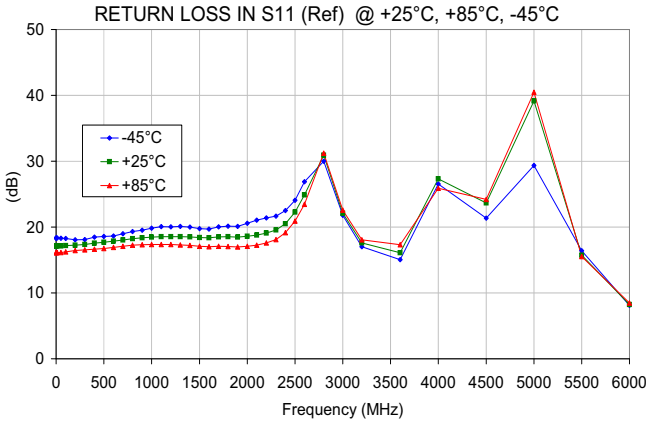
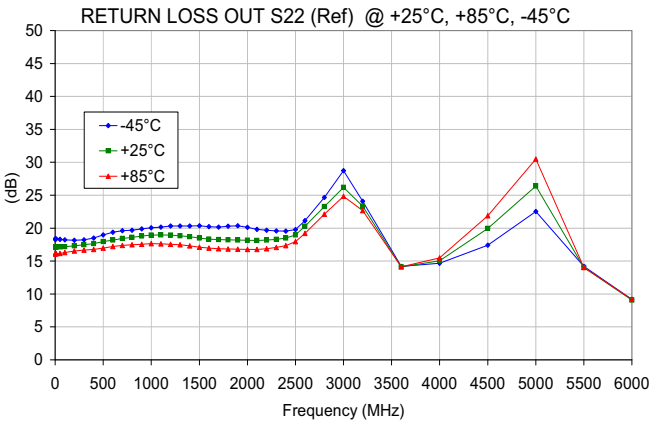
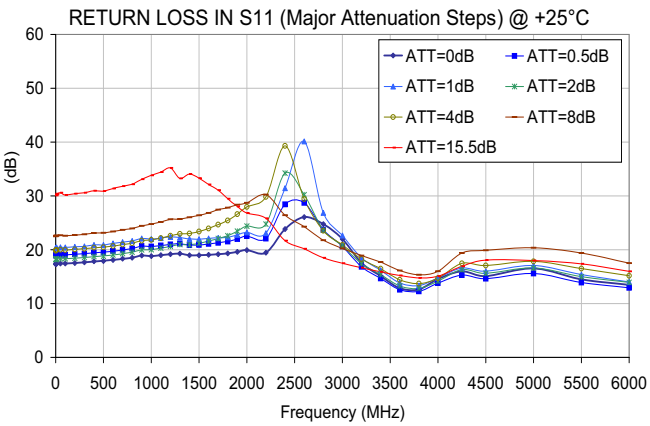
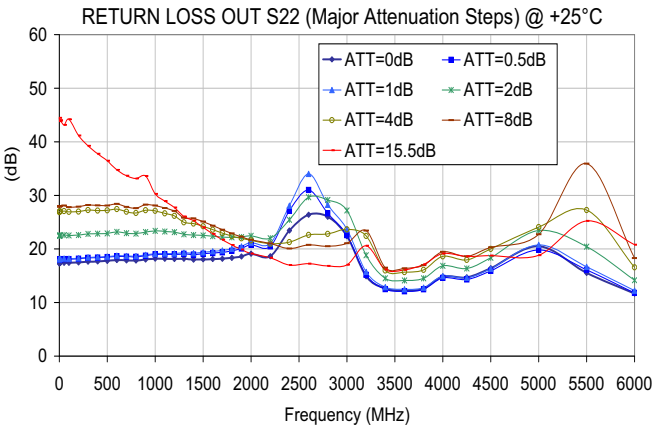
Typical Performance Curves











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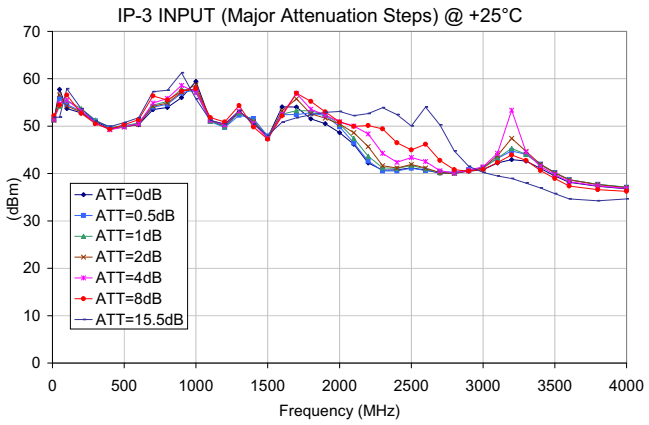

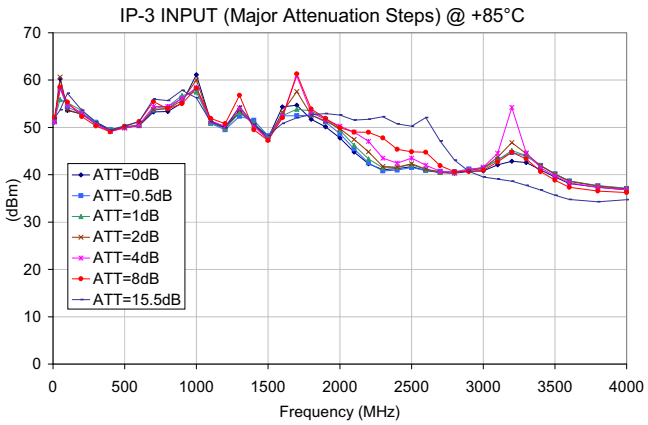

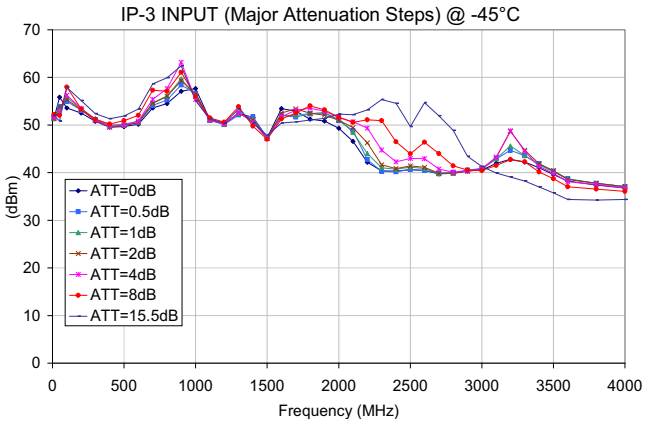

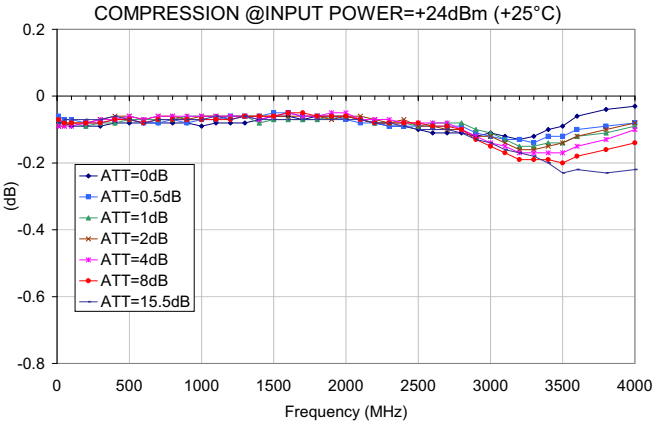

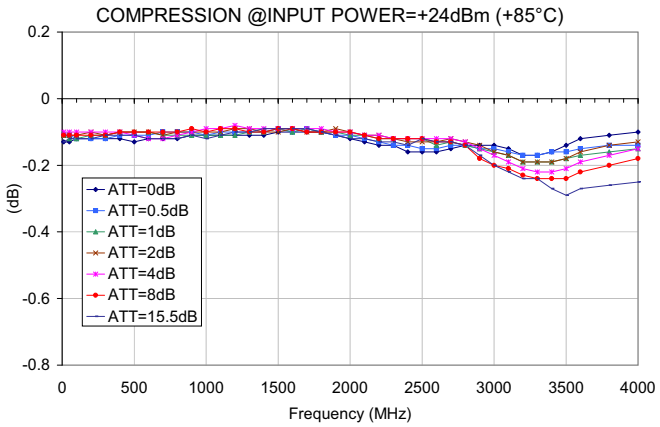

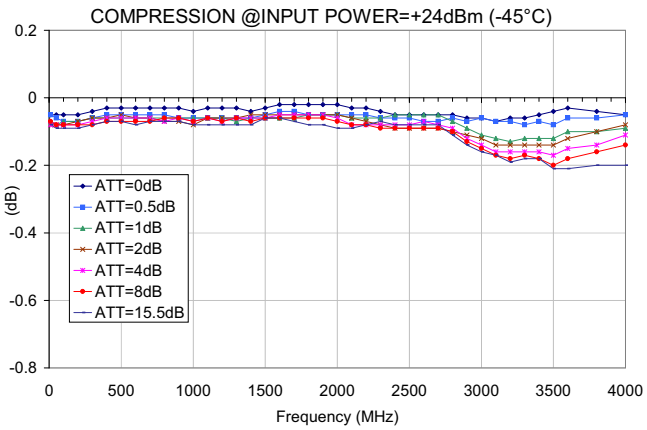

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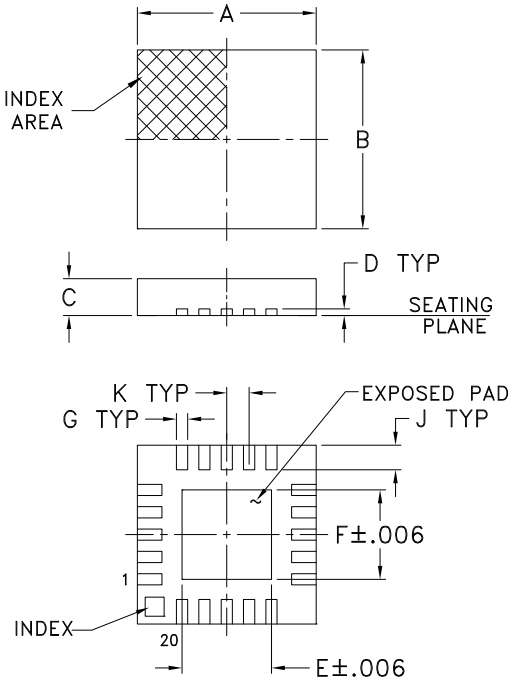
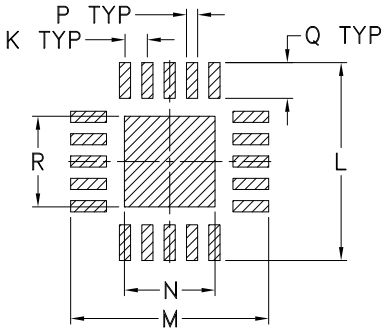
Outline Drawing (DG983-1)

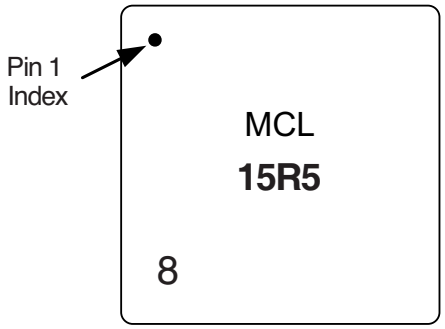


PCB Land Pattern



Suggested Layout,
Tolerance to be within ±.002

Device Marking



Outline Dimensions (inch)

A	B	C	D	E	F	G	H	J	K	˘	ˇ	ˆ	P	˙	˝	WT. GRAMS
.157	**.157**	**.035**	**.008**	**.081**	**.081**	**.010**	**—**	**.022**	**.020**	**.177**	**.177**	**.081**	**.010**	**.032**	**.081**	˜!"
"˜!!	"˜!!	!˜#!	0.20	2.06	2.06	0.25	%	0.56	!˜$!	"˜$!	"˜$!	2.06	0.25	!˜&	2.06	

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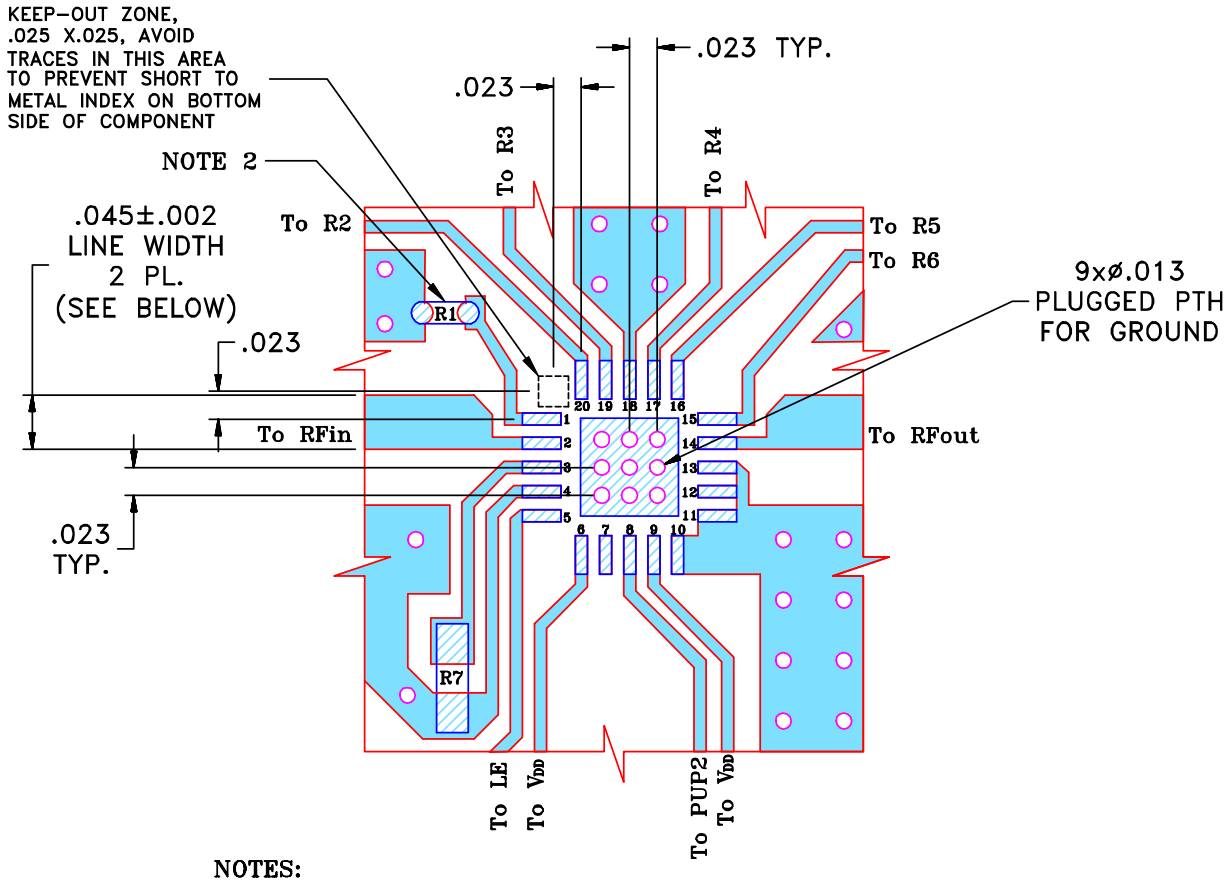
Suggested Layout for PCB Design (PL-197)

The suggested Layout shows only the footprint area of the DAT, and the components located near this area (i.e.: R1, R7). For the complete Layout, see photo and schematic diagram on page 11 of 12.



NOTES:

1. TRACE WIDTH IS SHOWN FOR FR4 WITH DIELECTRIC THICKNESS. .025"±.002". COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED.
2. 0603, 0402 SIZES CHIP FOOT PRINTS SHOWN FOR REFERENCE, VALUES OF RESISTORS WILL VARY BASED ON APPLICATION.
3. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.

DENOTES PCB COPPER LAYOUT WITH SMOBC (SOLDER MASK OVER BARE COPPER)

DENOTES COPPER LAND PATTERN FREE OF SOLDERMASK

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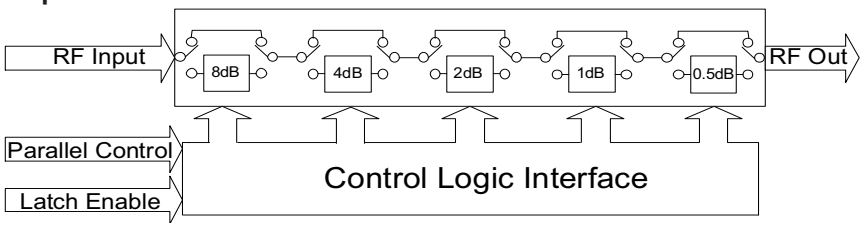
Simplified Schematic



The DAT-15R5-PP+ Parallel interface consists of 5 control bits that select the desired attenuation state, as shown in **Table 1**: Truth Table

Table 1. Truth Table

Attenuation State	C8	C4	C2	C1	C0.5
Reference	!	!	!	!	!
0.5 (dB)	!	!	!	!	
1 (dB)	!	!	!		!
2 (dB)	!	!		!	!
4 (dB)	!		!	!	!
8 (dB)		!	!	!	!
15.5 (dB)					

Note: Not all 32 possible combinations of C0.5 - C8 are shown in table

The parallel interface timing requirements are defined by Figure 1 (Parallel Interface Timing Diagram) and **Table 2** (Parallel Interface AC Characteristics), and switching speed.

For latched parallel programming the Latch Enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (per Figure 1) to latch new attenuation state into device.

For direct parallel programming, the Latch Enable (LE) line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct models is ideal for manual control of the device (using hardwire, switches, or jumpers).

Figure 1: Parallel Interface Timing Diagram

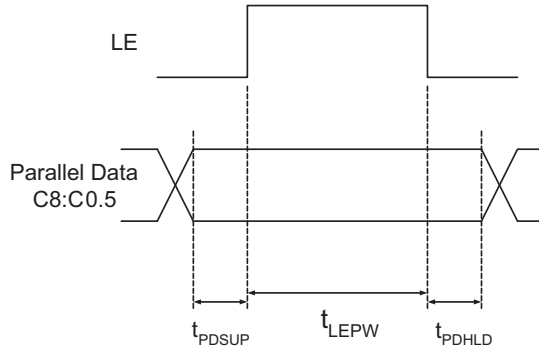


Table 2. Parallel Interface AC Characteristics

Symbol	Parameter	Min.	Max.	Units
)LEPW	LE minimum pulse 23*)4	!		/(
)PDSUP	Data set-up time before clock rising edge of LE	!		/(
)PDHLD	Data hold time after clock falling edge of LE	!		/(

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Pin 1 must always be low to prevent the attenuator from entering an unknown state.

Power-up Control Settings

The DAT-15R5-PP+ always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial parallel control word is provided.

When the attenuator powers up with LE=0, the control bits are automatically set to one of two possible values. These two values are selected by the power-up control bit, PUP2, as shown in Table B; (Power-Up Truth Table, Parallel Mode).

Table 3. Power-Up Truth Table, Parallel Mode

Attenuation State	PUP2	LE
Reference	!	!
8 (dB)		!
Defined by C0.5-C8 (See Table 1-Truth Table)	X (Note 1)	

Note 1: PUP2 Connection may be 0, 1, GROUND, or not connect, without effect on attenuation state.

Power-Up with LE=1 provides normal parallel operation with C0.5-C8, and PUP2 is not active.

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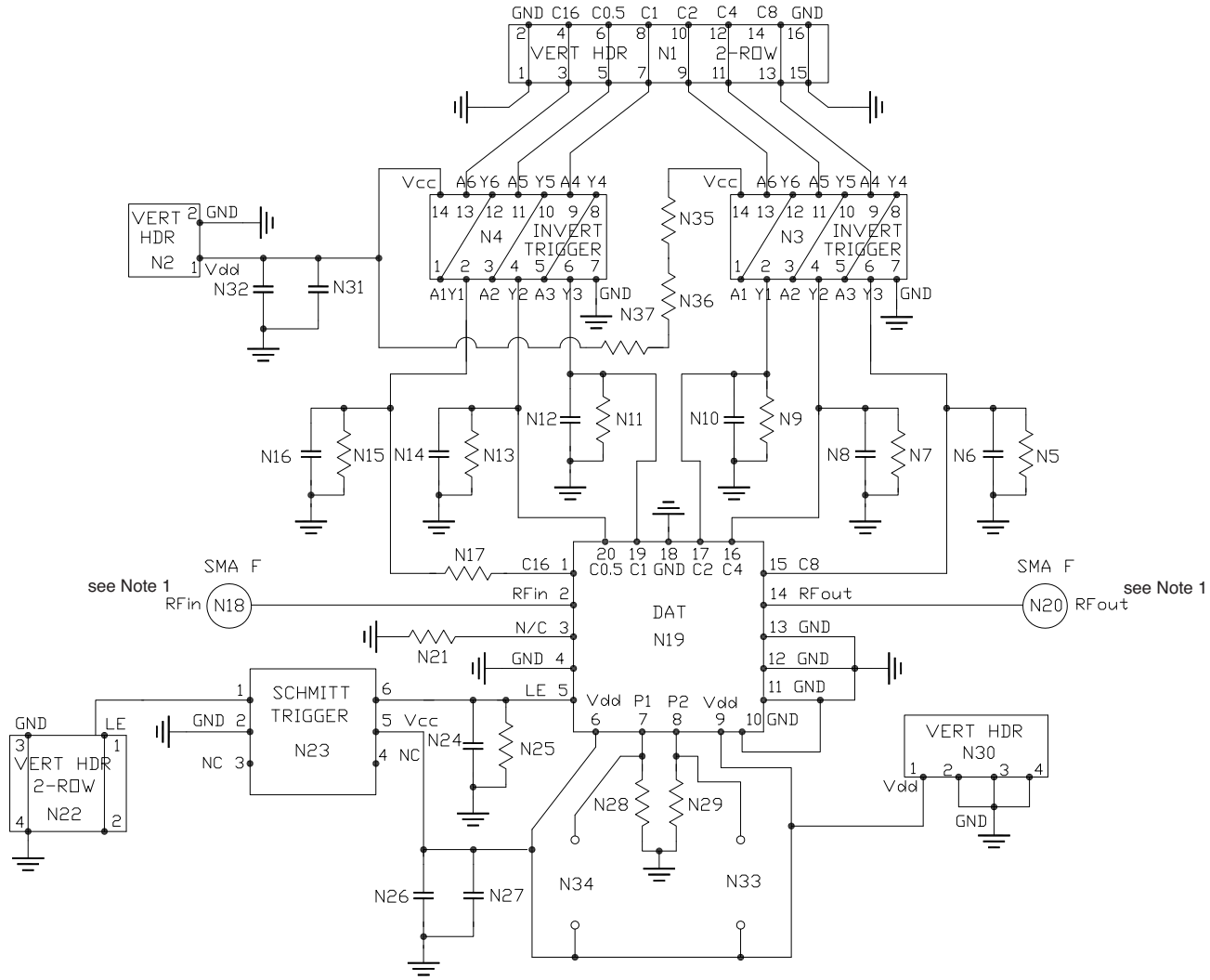
TB- 339 Evaluation Board Schematic Diagram



Note 1: Both RF ports must be held at 0VDC or DC blocked with an external series capacitor.

Bill of Materials	
N5, N7, N9, N11, N13, N15, N21 & N25	Resistor 0603 10 KOhm +/- 1%
N28 & N29	Resistor 0603 475 Ohm +/- 1%
N35 - N37	Resistor 0603 0 Ohm
N17	Resistor 0402 10 KOhm +/- 1%
N6, N8, N10, N12, N14, N16, N24, N26 & N32	NPO Capacitor 0603 100pF +/- 5%
N27 & N31	Tantalum Capacitor 0805 100nF +/- 10%
N3 & N4	Hex Invert Schmitt Trigger MSL1
N23	Dual Schmitt Trigger Buffer SC-70 MSL1

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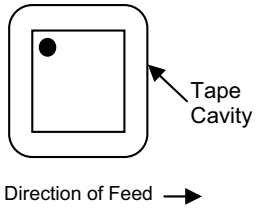
Tape and Reel Packaging Information

Table T&R

TR No.	No. of Devices	Reel Size	Tape Width	Pitch	Unit Orientation
F87	Small quantity standards 20, 50, 100, 200	7 inch	12 mm	8 mm	
	3000 (Standard)	13 inch			

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