

FEATURES

- 4.5 Ω typical on resistance
- 1 Ω on-resistance flatness
- Up to 206 mA continuous current
- ± 3.3 V to ± 8 V dual-supply operation
- 3.3 V to 16 V single-supply operation
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation

ADG1633

16-lead TSSOP and 16-lead, 3 mm \times 3 mm LFCSP

ADG1634

20-lead TSSOP and 20-lead, 4 mm \times 4 mm LFCSP

APPLICATIONS

- Communication systems
- Medical systems
- Audio signal routing
- Video signal routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Relay replacements

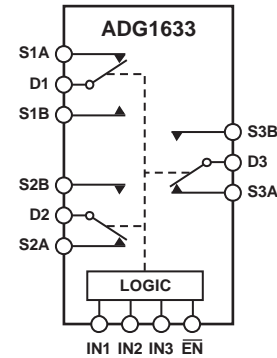
GENERAL DESCRIPTION

The [ADG1633](#) and [ADG1634](#) are monolithic industrial CMOS (*i*CMOS[®]) analog switches comprising three independently selectable single-pole, double-throw (SPDT) switches and four independently selectable SPDT switches, respectively.

All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An \overline{EN} input on the [ADG1633](#) (LFCSP and TSSOP packages) and [ADG1634](#) (LFCSP package only) is used to enable or disable the devices. When disabled, all channels are switched off.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications, where low distortion is critical. *i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

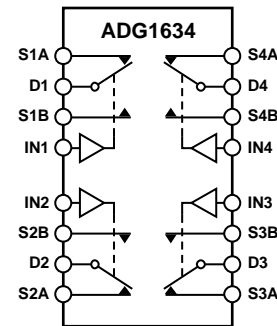
FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR
A 1 INPUT LOGIC.

08319-001

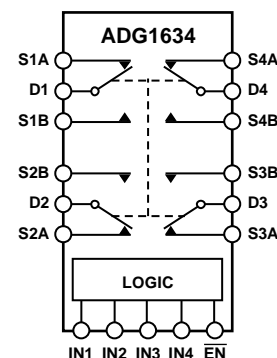
Figure 1. [ADG1633](#) TSSOP and LFCSP_VQ



SWITCHES SHOWN FOR
A 1 INPUT LOGIC.

08319-002

Figure 2. [ADG1634](#) TSSOP



SWITCHES SHOWN FOR
A 1 INPUT LOGIC.

08319-003

Figure 3. [ADG1634](#) LFCSP_VQ

Rev. A

[Document Feedback](#)

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REVISION HISTORY

9/14—Rev. 0 to Rev. A

| | |
|---|----|
| Changes to Figure 26, Figure 27, Figure 28..... | 14 |
| Updated Outline Dimensions | 17 |
| Changes to Ordering Guide | 19 |

7/09—Revision 0: Initial Version

SPECIFICATIONS

±5 V DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|------------|----------------|----------------------|-------------------|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | V_{DD} to V_{SS} | V | |
| On Resistance (R_{ON}) | 4.5 | | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26 |
| | 5 | 7 | 8 | Ω max | $V_{DD} = \pm 4.5\text{ V}$, $V_{SS} = \pm 4.5\text{ V}$ |
| On-Resistance Match Between Channels (ΔR_{ON}) | 0.12 | | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.25 | 0.3 | 0.35 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 1 | | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$ |
| | 1.3 | 1.7 | 2 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.01 | | | nA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | ± 0.1 | ± 1.5 | ± 12 | nA max | $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 27 |
| Drain Off Leakage, I_D (Off) | ± 0.02 | | | nA typ | $V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 27 |
| | ± 0.15 | ± 2 | ± 20 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.02 | | | nA typ | $V_S = V_D = \pm 4.5\text{ V}$; see Figure 28 |
| | ± 0.15 | ± 2 | ± 20 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | ± 1 | | | nA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 8 | | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{TRANSITION}$ | 161 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 200 | 236 | 264 | ns max | $V_S = 2.5\text{ V}$; see Figure 29 |
| $t_{ON}(\overline{EN})$ | 61 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 79 | 88 | 98 | ns max | $V_S = 2.5\text{ V}$; see Figure 31 |
| $t_{OFF}(\overline{EN})$ | 162 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 199 | 232 | 259 | ns max | $V_S = 2.5\text{ V}$; see Figure 31 |
| Break-Before-Make Time Delay, t_D | 44 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | | 30 | ns min | $V_{S1} = V_{S2} = 2.5\text{ V}$; see Figure 30 |
| Charge Injection | -12.5 | | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32 |
| Off Isolation | -64 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 33 |
| Channel-to-Channel Crosstalk | -64 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 35 |
| Total Harmonic Distortion + Noise (THD + N) | 0.3 | | | % typ | $R_L = 110\ \Omega$, $V_S = 5\text{ V p-p}$, $f = 20\text{ Hz}$ to 20 kHz ; see Figure 36 |
| -3 dB Bandwidth | 103 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 34 |
| C_S (Off) | 19 | | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| C_D (Off) | 33 | | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| C_D , C_S (On) | 57 | | | pF typ | $V_S = 0\text{ V}$, $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.001 | | | μA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | | | 1.0 | μA max | Digital inputs = 0 V or V_{DD} |
| V_{DD}/V_{SS} | | | $\pm 3.3/\pm 8$ | V min/max | |

¹ Guaranteed by design, but not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|------------|----------------|-----------------|-------------------|---|
| ANALOG SWITCH | | | | | |
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 4 | | | Ω typ | $V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$; see Figure 26 |
| | 4.5 | 6.5 | 7.5 | Ω max | $V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$ |
| On-Resistance Match Between Channels (ΔR_{ON}) | 0.12 | | | Ω typ | $V_S = 10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.25 | 0.3 | 0.35 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 0.9 | | | Ω typ | $V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$ |
| | 1.2 | 1.6 | 1.9 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| LEAKAGE CURRENTS | | | | | $V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$ |
| Source Off Leakage, I_S (Off) | ± 0.01 | | | nA typ | $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 27 |
| | ± 0.1 | ± 1.5 | ± 12 | nA max | |
| Drain Off Leakage, I_D (Off) | ± 0.02 | | | nA typ | $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 27 |
| | ± 0.15 | ± 2 | ± 20 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.02 | | | nA typ | $V_S = V_D = 1\text{ V}$ or 10 V ; see Figure 28 |
| | ± 0.15 | ± 2 | ± 20 | nA max | |
| DIGITAL INPUTS | | | | | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | ± 1 | | | nA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 8 | | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| DYNAMIC CHARACTERISTICS ¹ | | | | | |
| Transition Time, $t_{TRANSITION}$ | 127 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 151 | 182 | 205 | ns max | $V_S = 8\text{ V}$; see Figure 29 |
| $t_{ON}(\overline{EN})$ | 31 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 38 | 43 | 47 | ns max | $V_S = 8\text{ V}$; see Figure 31 |
| $t_{OFF}(\overline{EN})$ | 128 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 152 | 180 | 200 | ns max | $V_S = 8\text{ V}$; see Figure 31 |
| Break-Before-Make Time Delay, t_D | 45 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | | 30 | ns min | $V_{S1} = V_{S2} = 8\text{ V}$; see Figure 30 |
| Charge Injection | -12.4 | | | pC typ | $V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32 |
| Off Isolation | -64 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 33 |
| Channel-to-Channel Crosstalk | -64 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 35 |
| Total Harmonic Distortion + Noise (THD + N) | 0.3 | | | % typ | $R_L = 110\ \Omega$, $V_S = 5\text{ V}$ p-p, $f = 20\text{ Hz}$ to 20 kHz ; see Figure 36 |
| -3 dB Bandwidth | 109 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 34 |
| C_S (Off) | 19 | | | pF typ | $V_S = 6\text{ V}$, $f = 1\text{ MHz}$ |
| C_D (Off) | 32 | | | pF typ | $V_S = 6\text{ V}$, $f = 1\text{ MHz}$ |
| C_D , C_S (On) | 56 | | | pF typ | $V_S = 6\text{ V}$, $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| POWER REQUIREMENTS | | | | | $V_{DD} = 12\text{ V}$ |
| I_{DD} | 0.001 | | | μA typ | Digital inputs = 0 V or V_{DD} |
| | | | 1.0 | μA max | |
| TSSOP | 300 | | | μA typ | Digital inputs = 5 V |
| | | | 480 | μA max | |
| LFCSP | 375 | | | μA typ | Digital inputs = 5 V |
| | | | 600 | μA max | |
| V_{DD} | | | 3.3/16 | V min/max | |

¹ Guaranteed by design, but not subject to production test.

5 V SINGLE SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|------------|----------------|-----------------|-------------------|--|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 8.5 | | | Ω typ | $V_S = 0\text{ V to }4.5\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26 |
| | 10 | 12.5 | 14 | Ω max | $V_{DD} = 4.5\text{ V}$, $V_{SS} = 0\text{ V}$ |
| On-Resistance Match Between Channels (ΔR_{ON}) | 0.15 | | | Ω typ | $V_S = 0\text{ V to }4.5\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.3 | 0.35 | 0.4 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 1.7 | | | Ω typ | $V_S = 0\text{ V to }4.5\text{ V}$, $I_S = -10\text{ mA}$ |
| | 2.3 | 2.7 | 3 | Ω max | |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.01 | | | nA typ | $V_{DD} = 5.5\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 27 |
| | ± 0.1 | ± 1.5 | ± 12 | nA max | |
| Drain Off Leakage, I_D (Off) | ± 0.02 | | | nA typ | $V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$; see Figure 27 |
| | ± 0.15 | ± 2 | ± 20 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.02 | | | nA typ | $V_S = V_D = 1\text{ V or }4.5\text{ V}$; see Figure 28 |
| | ± 0.15 | ± 2 | ± 20 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | ± 1 | | | nA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | | ± 0.1 | $\mu\text{A max}$ | |
| Digital Input Capacitance, C_{IN} | 8 | | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{TRANSITION}$ | 199 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 254 | 303 | 337 | ns max | $V_S = 2.5\text{ V}$; see Figure 29 |
| $t_{ON}(\overline{EN})$ | 68 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 90 | 102 | 110 | ns max | $V_S = 2.5\text{ V}$; see Figure 31 |
| $t_{OFF}(\overline{EN})$ | 201 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 256 | 300 | 333 | ns max | $V_S = 2.5\text{ V}$; see Figure 31 |
| Break-Before-Make Time Delay, t_D | 57 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | | 37 | ns min | $V_{S1} = V_{S2} = 2.5\text{ V}$; see Figure 30 |
| Charge Injection | -5 | | | pC typ | $V_S = 2.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32 |
| Off Isolation | -64 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 33 |
| Channel-to-Channel Crosstalk | -64 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 35 |
| Total Harmonic Distortion + Noise (THD + N) | 0.27 | | | % typ | $R_L = 110\ \Omega$, $f = 20\text{ Hz to }20\text{ kHz}$, $V_S = 3.5\text{ V p-p}$; see Figure 36 |
| -3 dB Bandwidth | 104 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 34 |
| C_S (Off) | 21 | | | pF typ | $V_S = 2.5\text{ V}$, $f = 1\text{ MHz}$ |
| C_D (Off) | 37 | | | pF typ | $V_S = 2.5\text{ V}$, $f = 1\text{ MHz}$ |
| C_D , C_S (On) | 62 | | | pF typ | $V_S = 2.5\text{ V}$, $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.001 | | | $\mu\text{A typ}$ | $V_{DD} = 5.5\text{ V}$ Digital inputs = 0 V or V_{DD} |
| | | | 1.0 | $\mu\text{A max}$ | |
| V_{DD} | | | 3.3/16 | V min/max | |

¹ Guaranteed by design, but not subject to production test.

3.3 V SINGLE SUPPLY

$V_{DD} = 3.3\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 4.

| Parameter | 25°C | -40°C to +85°C | -40°C to +125°C | Unit | Test Conditions/Comments |
|--|------------|-------------------|--------------------|-------------------|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 13.5 | 15 | 16.5 | Ω typ | $V_S = 0\text{ V to }V_{DD}$, $I_S = -10\text{ mA}$; see Figure 26, $V_{DD} = 3.3\text{ V}$, $V_{SS} = 0\text{ V}$ |
| On-Resistance Match Between Channels (ΔR_{ON}) | 0.25 | 0.28 | 0.3 | Ω typ | $V_S = 0\text{ V to }V_{DD}$, $I_S = -10\text{ mA}$ |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 5 | 5.5 | 6.5 | Ω typ | $V_S = 0\text{ V to }V_{DD}$, $I_S = -10\text{ mA}$ |
| LEAKAGE CURRENTS | | | | | |
| Source Off Leakage, I_S (Off) | ± 0.01 | | | nA typ | $V_{DD} = 3.6\text{ V}$, $V_{SS} = 0\text{ V}$ |
| | ± 0.1 | ± 1.5 | ± 12 | nA max | $V_S = 0.6\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/0.6\text{ V}$; see Figure 27 |
| Drain Off Leakage, I_D (Off) | ± 0.01 | | | nA typ | $V_S = 0.6\text{ V}/3\text{ V}$, $V_D = 3\text{ V}/0.6\text{ V}$; see Figure 27 |
| | ± 0.15 | ± 2 | ± 20 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.01 | | | nA typ | $V_S = V_D = 0.6\text{ V or }3\text{ V}$; see Figure 28 |
| | ± 0.15 | ± 2 | ± 20 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, V_{INH} | | | 2.0 | V min | |
| Input Low Voltage, V_{INL} | | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | ± 1 | | | nA typ | $V_{IN} = V_{GND}$ or V_{DD} |
| | | | ± 0.1 | $\mu\text{A max}$ | |
| Digital Input Capacitance, C_{IN} | 8 | | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | | |
| Transition Time, $t_{TRANSITION}$ | 309 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 429 | 466 | 508 | ns max | $V_S = 1.5\text{ V}$; see Figure 29 |
| $t_{ON}(\overline{EN})$ | 132 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 184 | 201 | 210 | ns max | $V_S = 1.5\text{ V}$; see Figure 31 |
| $t_{OFF}(\overline{EN})$ | 313 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 416 | 470 | 509 | ns max | $V_S = 1.5\text{ V}$; see Figure 31 |
| Break-Before-Make Time Delay, t_D | 81 | | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | | | 48 | ns min | $V_{S1} = V_{S2} = 1.5\text{ V}$; see Figure 30 |
| Charge Injection | -10 | | | pC typ | $V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 32 |
| Off Isolation | -64 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 33 |
| Channel-to-Channel Crosstalk | -64 | | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 35 |
| Total Harmonic Distortion + Noise (THD + N) | 0.6 | | | % typ | $R_L = 110\ \Omega$, $f = 20\text{ Hz to }20\text{ kHz}$, $V_S = 2\text{ V p-p}$; see Figure 36 |
| -3 dB Bandwidth | 117 | | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 34 |
| C_S (Off) | 22 | | | pF typ | $V_S = 1.5\text{ V}$, $f = 1\text{ MHz}$ |
| C_D (Off) | 39 | | | pF typ | $V_S = 1.5\text{ V}$, $f = 1\text{ MHz}$ |
| C_D , C_S (On) | 64 | | | pF typ | $V_S = 1.5\text{ V}$, $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | | |
| I_{DD} | 0.001 | | | $\mu\text{A typ}$ | $V_{DD} = 3.6\text{ V}$ |
| | | | 1.0 | $\mu\text{A max}$ | Digital inputs = 0 V or V_{DD} |
| V_{DD} | | | 3.3/16 | V min/max | |

¹ Guaranteed by design, but not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D**Table 5. ADG1633**

| Parameter | 25°C | 85°C | 125°C | Unit |
|---|------|------|-------|--------|
| CONTINUOUS CURRENT, S OR D | | | | |
| $V_{DD} = +5\text{ V}, V_{SS} = -5\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$) | 126 | 84 | 56 | mA max |
| LFCSP ($\theta_{JA} = 48.7^\circ\text{C/W}$) | 206 | 126 | 70 | mA max |
| $V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$) | 133 | 87 | 56 | mA max |
| LFCSP ($\theta_{JA} = 48.7^\circ\text{C/W}$) | 213 | 133 | 73 | mA max |
| $V_{DD} = 5\text{ V}, V_{SS} = 0\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$) | 98 | 70 | 45 | mA max |
| LFCSP ($\theta_{JA} = 48.7^\circ\text{C/W}$) | 157 | 105 | 63 | mA max |
| $V_{DD} = 3.3\text{ V}, V_{SS} = 0\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$) | 77 | 56 | 38 | mA max |
| LFCSP ($\theta_{JA} = 48.7^\circ\text{C/W}$) | 129 | 87 | 56 | mA max |

Table 6. ADG1634

| Parameter | 25°C | 85°C | 125°C | Unit |
|--|------|------|-------|--------|
| CONTINUOUS CURRENT, S OR D | | | | |
| $V_{DD} = +5\text{ V}, V_{SS} = -5\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 95^\circ\text{C/W}$) | 112 | 77 | 52 | mA max |
| LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$) | 220 | 136 | 73 | mA max |
| $V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 95^\circ\text{C/W}$) | 119 | 80 | 52 | mA max |
| LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$) | 234 | 140 | 73 | mA max |
| $V_{DD} = 5\text{ V}, V_{SS} = 0\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 95^\circ\text{C/W}$) | 87 | 63 | 42 | mA max |
| LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$) | 171 | 112 | 66 | mA max |
| $V_{DD} = 3.3\text{ V}, V_{SS} = 0\text{ V}$ | | | | |
| TSSOP ($\theta_{JA} = 95^\circ\text{C/W}$) | 70 | 52 | 35 | mA max |
| LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$) | 140 | 94 | 59 | mA max |

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 7.

| Parameter | Rating |
|---|--|
| V_{DD} to V_{SS} | 18 V |
| V_{DD} to GND | -0.3 V to +18 V |
| V_{SS} to GND | +0.3 V to -18 V |
| Analog Inputs ¹ | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Digital Inputs ¹ | GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Peak Current, S or D | 450 mA (pulsed at 1 ms, 10% duty cycle maximum) |
| Continuous Current, S or D ² | Data + 15% |
| Operating Temperature Range Industrial (Y Version) | -40°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| 16-Lead TSSOP, θ_{JA} Thermal Impedance, 0 Airflow (4- Layer Board) | 112.6°C/W |
| 20-Lead TSSOP, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board) | 95°C/W |
| 16-Lead LFCSP (3 mm × 3 mm), θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board) | 48.7°C/W |
| 16-Lead LFCSP (4 mm × 4 mm), θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board) | 30.4°C/W |
| Reflow Soldering Peak Temperature, Pb free | 260°C |

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

² See Table 5 and Table 6.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

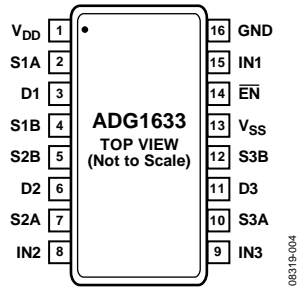
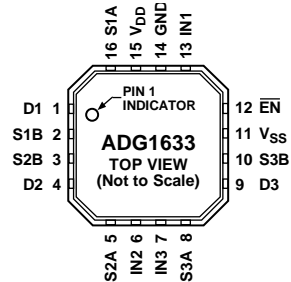


Figure 4. ADG1633 TSSOP Pin Configuration



NOTES
1. EXPOSED PAD IS TIED TO THE SUBSTRATE, V_{SS} .

Figure 5. ADG1633 LFCSP_VQ Pin Configuration

Table 8. ADG1633 Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|---------|----------|-----------------|---|
| TSSOP | LFCSP_VQ | | |
| 1 | 15 | V_{DD} | Most Positive Power Supply Potential. |
| 2 | 16 | S1A | Source Terminal 1A. Can be an input or an output. |
| 3 | 1 | D1 | Drain Terminal 1. Can be an input or an output. |
| 4 | 2 | S1B | Source Terminal 1B. Can be an input or an output. |
| 5 | 3 | S2B | Source Terminal 2B. Can be an input or an output. |
| 6 | 4 | D2 | Drain Terminal 2. Can be an input or an output. |
| 7 | 5 | S2A | Source Terminal 2A. Can be an input or an output. |
| 8 | 6 | IN2 | Logic Control Input 2. |
| 9 | 7 | IN3 | Logic Control Input 3. |
| 10 | 8 | S3A | Source Terminal 3A. Can be an input or an output. |
| 11 | 9 | D3 | Drain Terminal 3. Can be an input or an output. |
| 12 | 10 | S3B | Source Terminal 3B. Can be an input or an output. |
| 13 | 11 | V_{SS} | Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground. |
| 14 | 12 | \overline{EN} | Active Low Digital Input. When this pin is high, the device is disabled and all switches are off. When this pin is low, INx logic inputs determine the on switches. |
| 15 | 13 | IN1 | Logic Control Input 1. |
| 16 | 14 | GND | Ground (0 V) Reference. |
| N/A | 17 | EP | Exposed Pad. The exposed pad is tied to the substrate, V_{SS} . |

Table 9. ADG1633 Truth Table

| \overline{EN} | INx | SxA | SxB |
|-----------------|----------------|-----|-----|
| 1 | X ¹ | Off | Off |
| 0 | 0 | Off | On |
| 0 | 1 | On | Off |

¹ X = don't care.

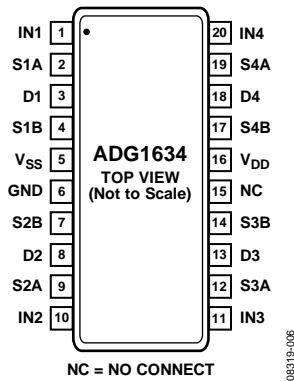
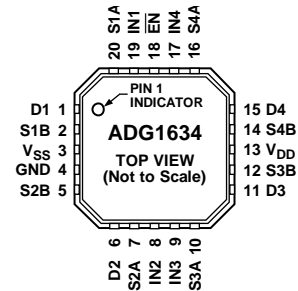


Figure 6. ADG1634 TSSOP Pin Configuration



NOTES
1. EXPOSED PAD IS TIED TO THE SUBSTRATE, V_{SS} .

Figure 7. ADG1634 LFCSP_VQ Pin Configuration

Table 10. ADG1634 Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|---------|----------|-----------------|---|
| TSSOP | LFCSP_VQ | | |
| 1 | 19 | IN1 | Logic Control Input 1. |
| 2 | 20 | S1A | Source Terminal 1A. Can be an input or an output. |
| 3 | 1 | D1 | Drain Terminal 1. Can be an input or an output. |
| 4 | 2 | S1B | Source Terminal 1B. Can be an input or an output. |
| 5 | 3 | V_{SS} | Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground. |
| 6 | 4 | GND | Ground (0 V) Reference. |
| 7 | 5 | S2B | Source Terminal 2B. Can be an input or an output. |
| 8 | 6 | D2 | Drain Terminal 2. Can be an input or an output. |
| 9 | 7 | S2A | Source Terminal 2A. Can be an input or an output. |
| 10 | 8 | IN2 | Logic Control Input 2. |
| 11 | 9 | IN3 | Logic Control Input 3. |
| 12 | 10 | S3A | Source Terminal 3A. Can be an input or an output. |
| 13 | 11 | D3 | Drain Terminal 3. Can be an input or an output. |
| 14 | 12 | S3B | Source Terminal 3B. Can be an input or an output. |
| 15 | N/A | NC | No Connect. |
| 16 | 13 | V_{DD} | Most Positive Power Supply Potential. |
| 17 | 14 | S4B | Source Terminal 4B. Can be an input or an output. |
| 18 | 15 | D4 | Drain Terminal 4. Can be an input or an output. |
| 19 | 16 | S4A | Source Terminal 4A. Can be an input or an output. |
| 20 | 17 | IN4 | Logic Control Input 4. |
| N/A | 18 | \overline{EN} | Active Low Digital Input. When this pin is high, the device is disabled and all switches are off. When this pin is low, INx logic inputs determine the on switches. |
| N/A | 21 | EP | Exposed Pad. The exposed pad is tied to the substrate, V_{SS} . |

Table 11. ADG1634 TSSOP Truth Table

| INx | SxA | SxB |
|-----|-----|-----|
| 0 | Off | On |
| 1 | On | Off |

Table 12. ADG1634 LFCSP_VQ Truth Table

| \overline{EN} | INx | SxA | SxB |
|-----------------|----------------|-----|-----|
| 1 | X ¹ | Off | Off |
| 0 | 0 | Off | On |
| 0 | 1 | On | Off |

¹ X = don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

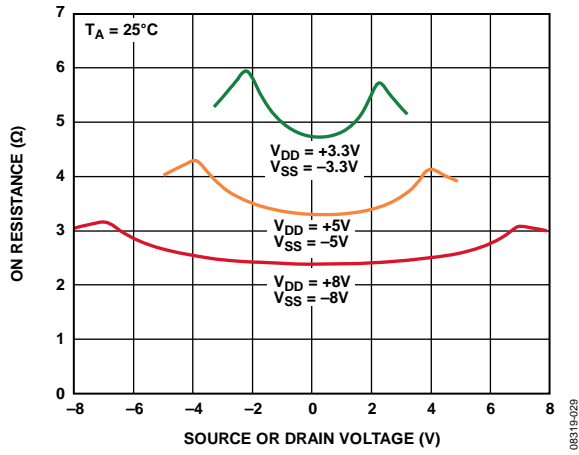


Figure 8. On Resistance vs. V_D (V_s), Dual Supply

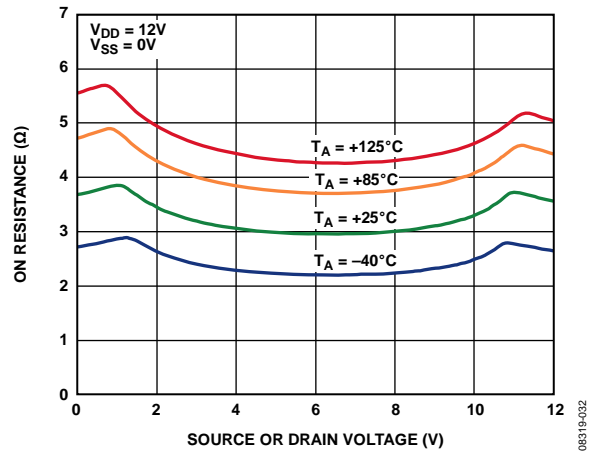


Figure 11. On Resistance vs. V_D (V_s) for Different Temperatures, 12 V Single Supply

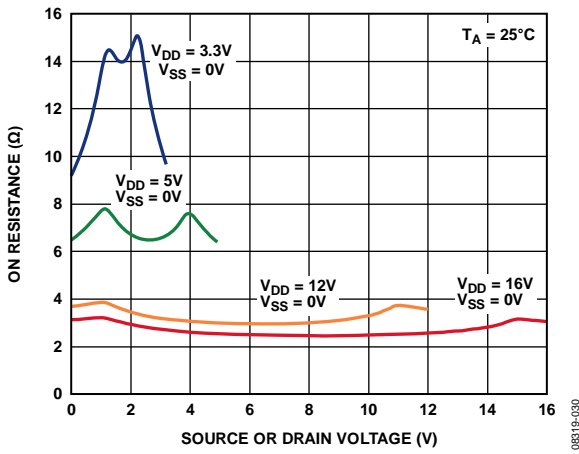


Figure 9. On Resistance vs. V_D (V_s), Single Supply

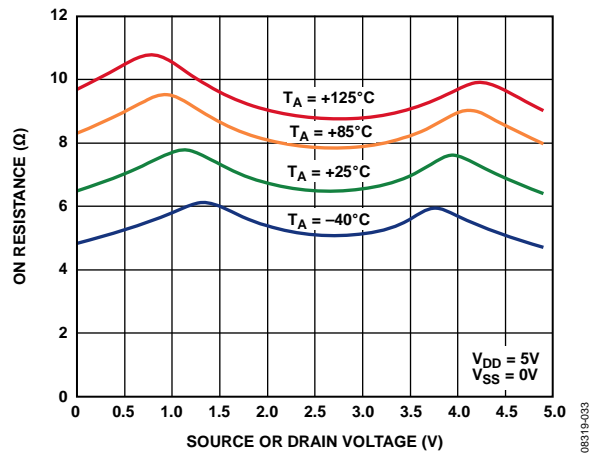


Figure 12. On Resistance vs. V_D (V_s) for Different Temperatures, 5 V Single Supply

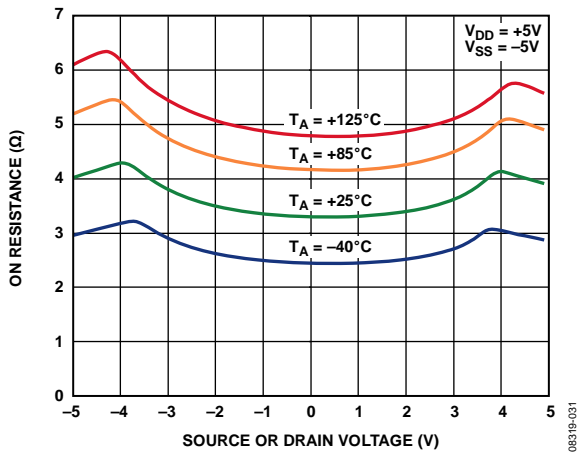


Figure 10. On Resistance vs. V_D (V_s) for Different Temperatures, ± 5 V Dual Supply

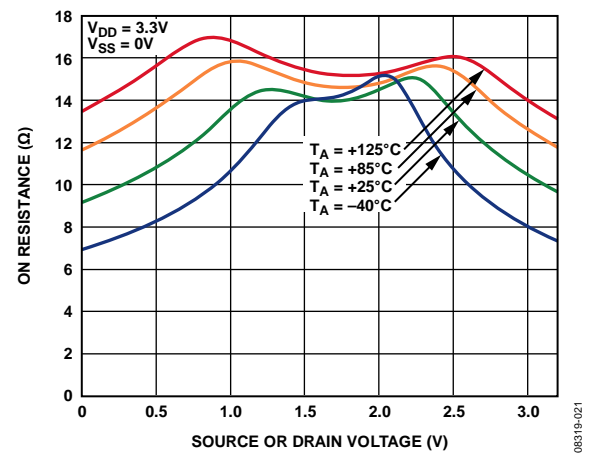


Figure 13. On Resistance vs. V_D (V_s) for Different Temperatures, 3.3 V Single Supply

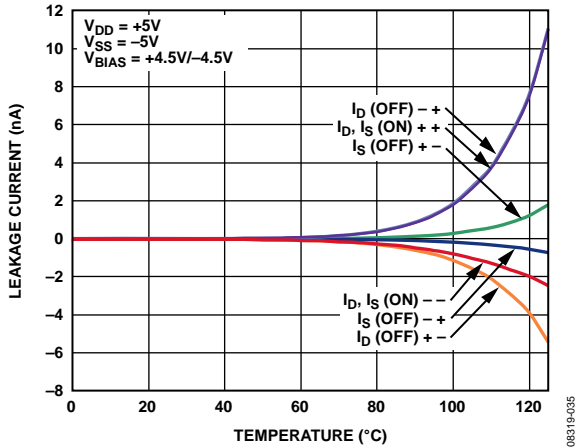


Figure 14. ADG1633 Leakage Currents vs. Temperature, ±5V Dual Supply

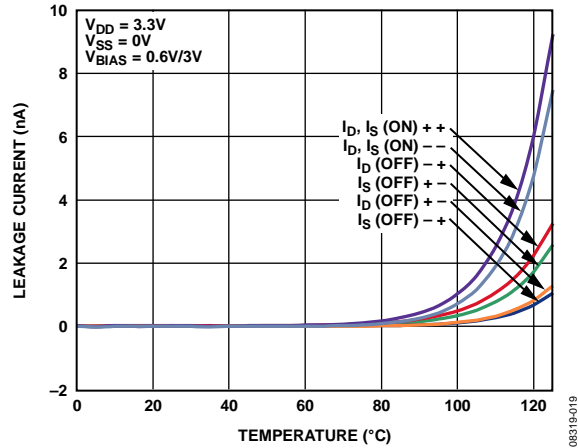


Figure 17. ADG1633 Leakage Currents vs. Temperature, 3.3V Single Supply

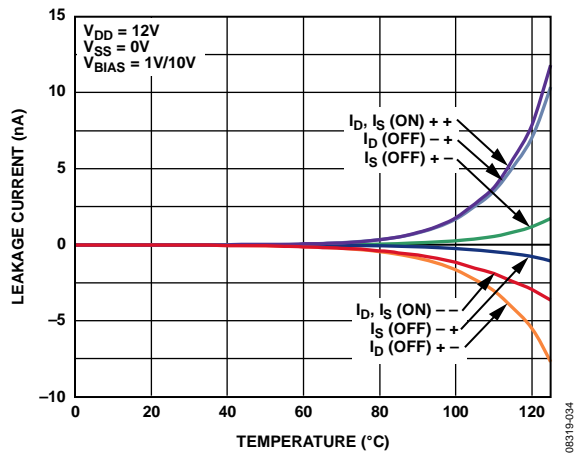


Figure 15. ADG1633 Leakage Currents vs. Temperature, 12V Single Supply

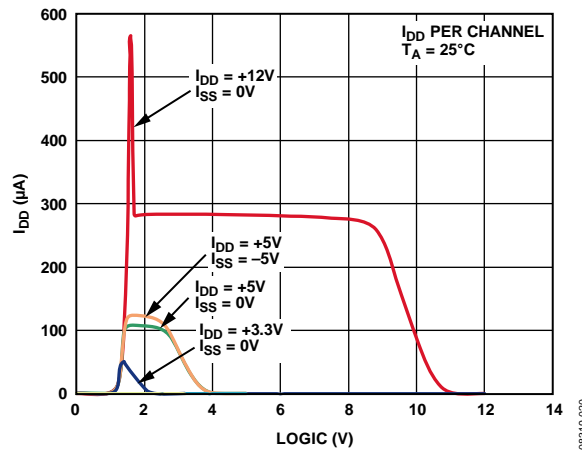


Figure 18. I_{DD} vs. Logic Level

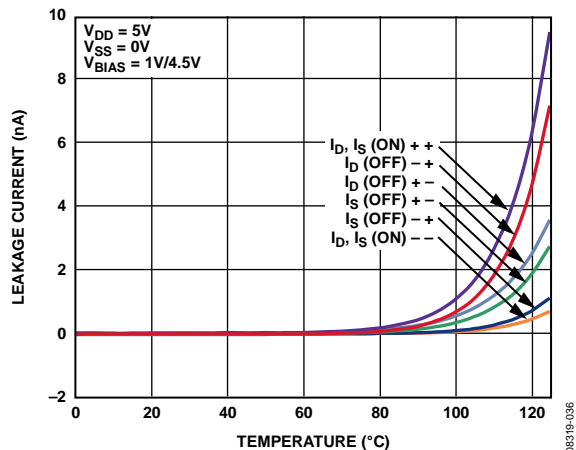


Figure 16. ADG1633 Leakage Currents vs. Temperature, 5V Single Supply

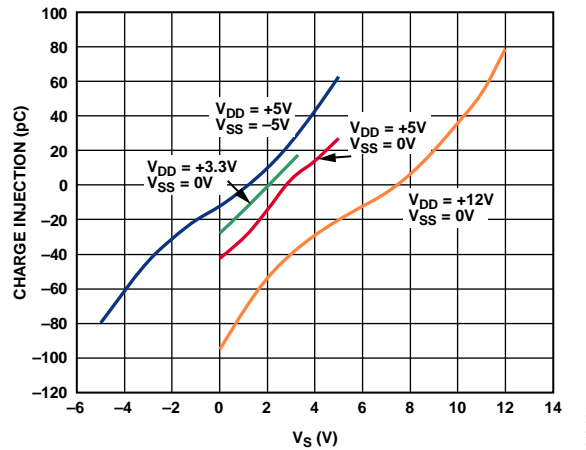


Figure 19. Charge Injection vs. Source Voltage

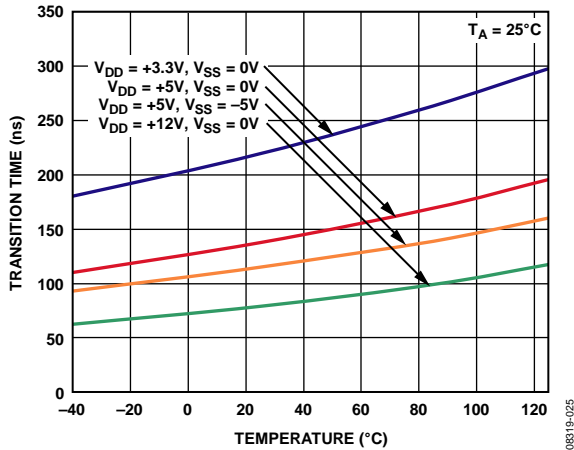


Figure 20. Transition Time vs. Temperature

08319-025

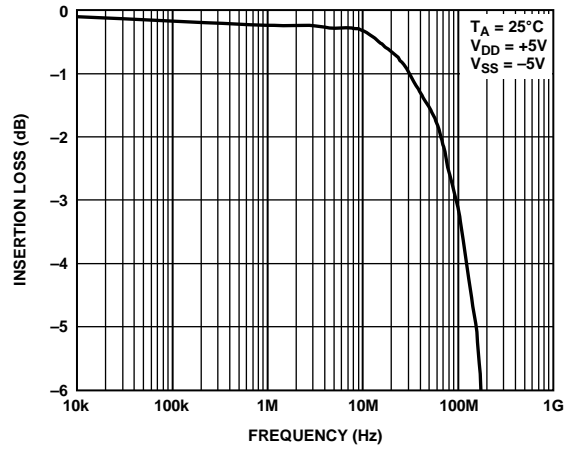


Figure 23. On Response vs. Frequency

08319-022

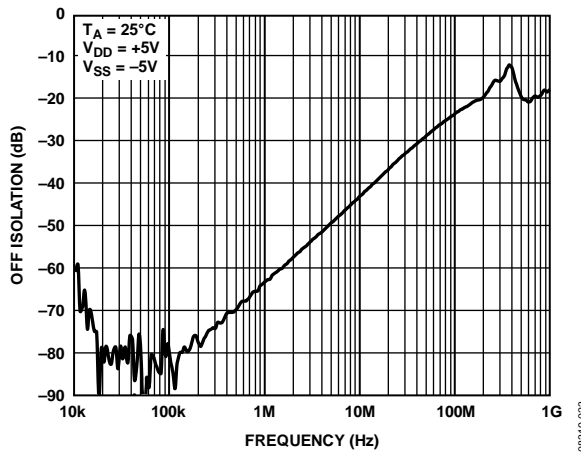


Figure 21. Off Isolation vs. Frequency

08319-023

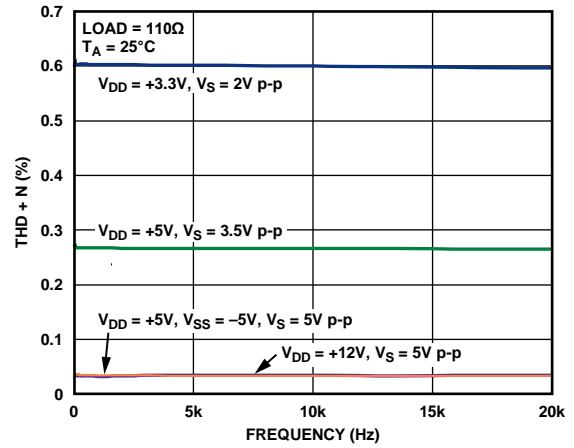


Figure 24. THD + N vs. Frequency

08319-028

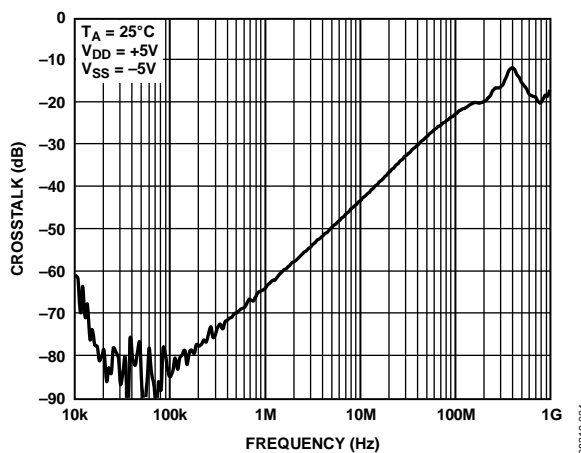


Figure 22. Crosstalk vs. Frequency

08319-024

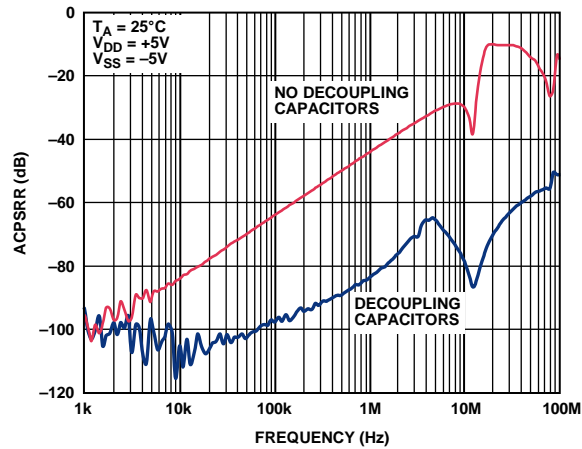


Figure 25. ACPSRR vs. Frequency

08319-026

TEST CIRCUITS

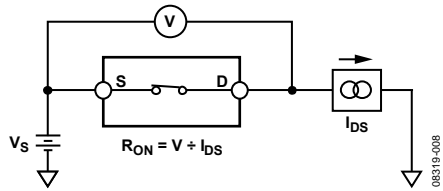


Figure 26. On Resistance

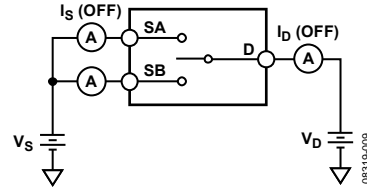


Figure 27. Off Leakage

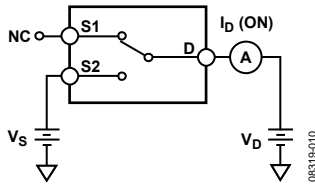


Figure 28. On Leakage

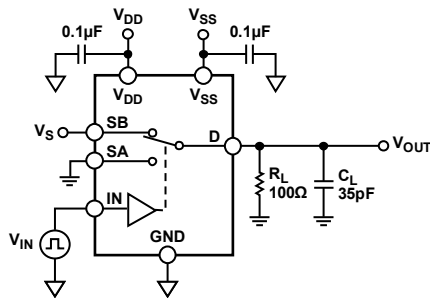


Figure 29. Switching Timing

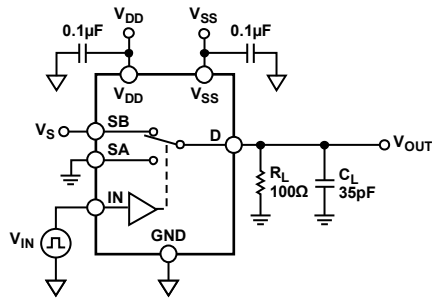


Figure 30. Break-Before-Make Delay, t_D

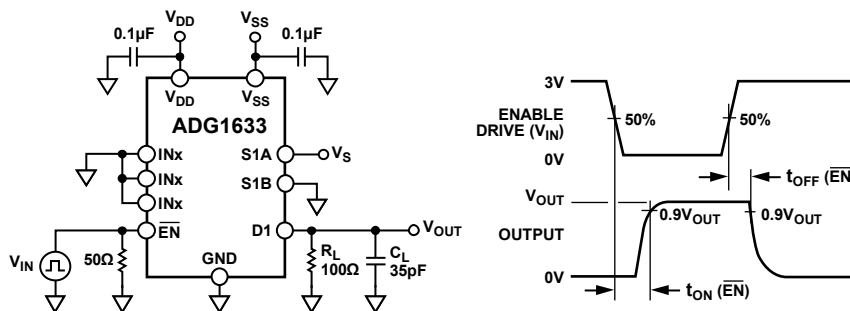


Figure 31. Enable Delay, $t_{ON}(\overline{EN})$, $t_{OFF}(\overline{EN})$

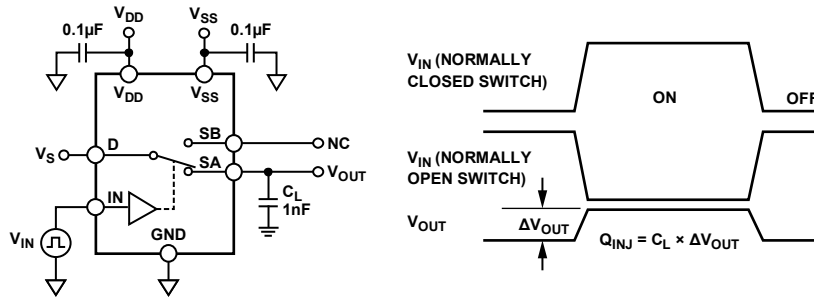


Figure 32. Charge Injection

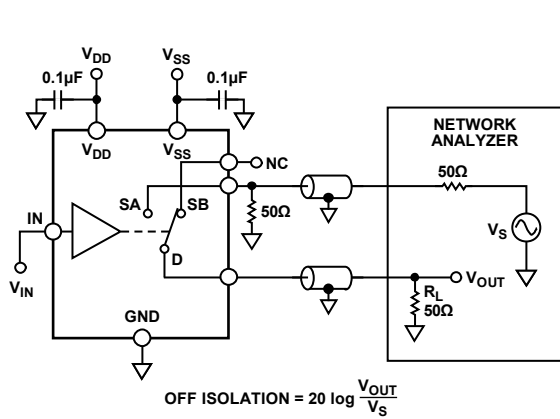


Figure 33. Off Isolation

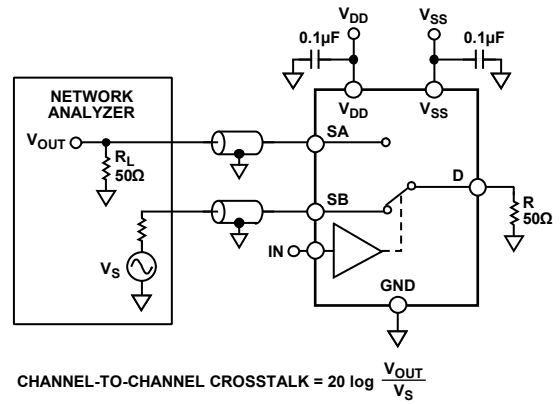


Figure 35. Channel-to-Channel Crosstalk

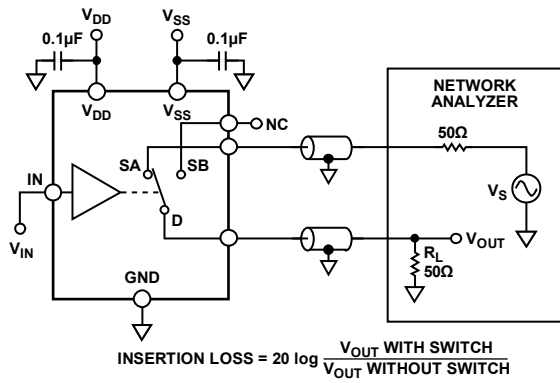


Figure 34. Bandwidth

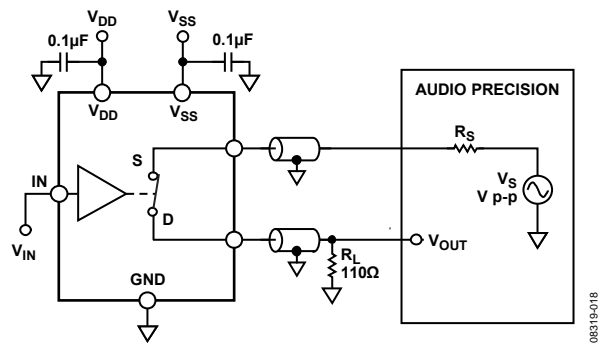


Figure 36. THD + Noise

TERMINOLOGY

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

The difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

The difference between the maximum and minimum value of on resistance measured.

I_S (Off)

Source leakage current when the switch is off.

I_D (Off)

Drain leakage current when the switch is off.

I_D, I_S (On)

Channel leakage current when the switch is on.

V_D (V_S)

Analog voltage on Terminal D and Terminal S.

C_S (Off)

Channel input capacitance for off condition.

C_D (Off)

Channel output capacitance for off condition.

C_D, C_S (On)

On switch capacitance.

C_{IN}

Digital input capacitance.

t_{ON} (\overline{EN})

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (\overline{EN})

Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{TRANS}

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{BBM}

Off time measured between the 80% point of both switches when switching from one address state to another.

V_{IL}

Maximum input voltage for Logic 0.

V_{IH}

Minimum input voltage for Logic 1.

I_{IL} (I_{IH})

Input current of the digital input.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

Off Isolation

A measure of unwanted signal coupling through an off channel.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

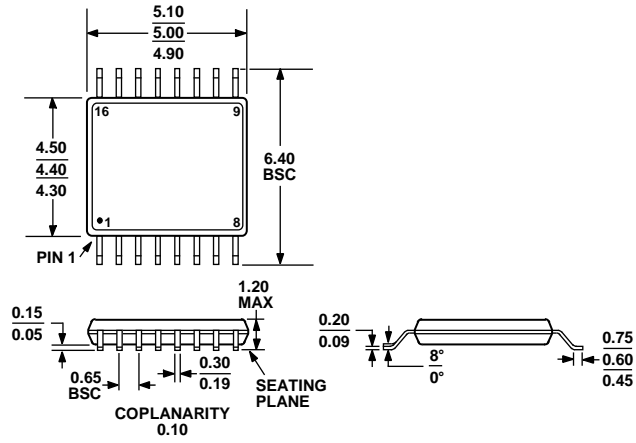
Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

A measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

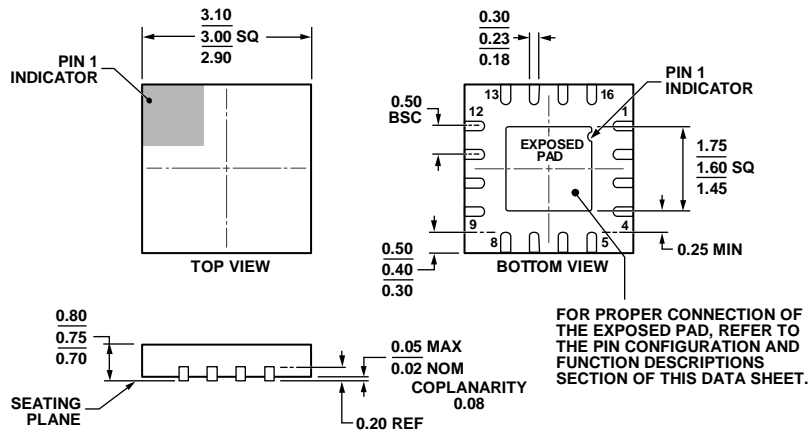
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 37. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters

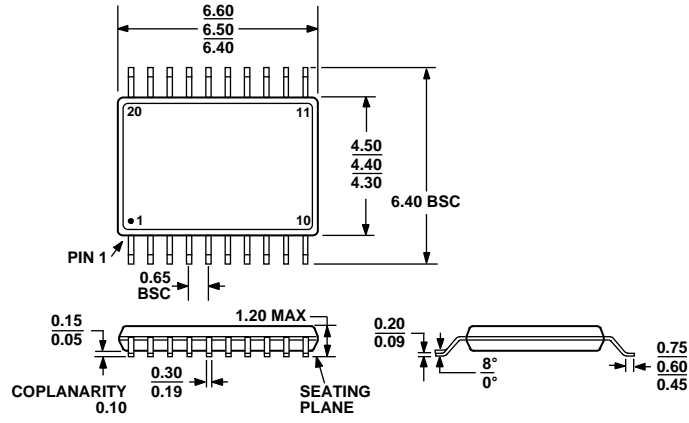


COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] 3 mm x 3 mm, Very VeryThin Quad (CP-16-22)

Dimensions shown in millimeters

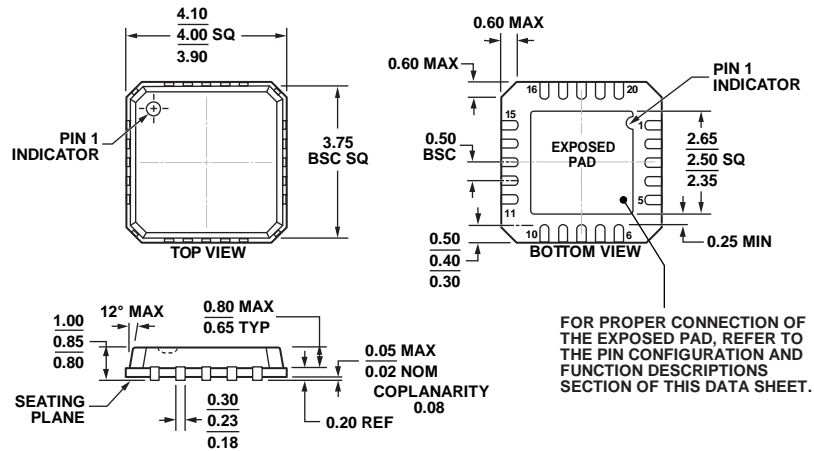
08-16-2010-E



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 39. 20-Lead Thin Shrink Small Outline Package [TSSOP] (RU-20)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 40. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ] 4 mm x 4 mm Body, Very Thin Quad (CP-20-4)

Dimensions shown in millimeters

04-09-2012-B

ORDERING GUIDE

| Model ¹ | Temperature Range | Description | $\overline{\text{EN}}$ Pin | Package Option | Branding |
|--------------------|-------------------|---|----------------------------|----------------|----------|
| ADG1633BRUZ | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | Yes | RU-16 | |
| ADG1633BRUZ-REEL7 | -40°C to +125°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | Yes | RU-16 | |
| ADG1633BCPZ-REEL7 | -40°C to +125°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | Yes | CP-16-22 | SD3 |
| ADG1634BRUZ | -40°C to +125°C | 20-Lead Thin Shrink Small Outline Package [TSSOP] | No | RU-20 | |
| ADG1634BRUZ-REEL7 | -40°C to +125°C | 20-Lead Thin Shrink Small Outline Package [TSSOP] | No | RU-20 | |
| ADG1634BCPZ-REEL7 | -40°C to +125°C | 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | Yes | CP-20-4 | |

¹Z = RoHS Compliant Part.

NOTES