Part Number: IB1416S650

Integra
TECHNOLOGIES, INC.

L-Band Avionics Transistor

The high power pulsed avionics transistor part number IB1416S650 is designed for L-Band avionics systems operating at 1450 to 1550 MHz. While operating in class C mode under (0.5μs ON, 1.5μs off) x 50, 1%, pulse conditions at V_{CC}= 50V, this common base device supplies a minimum of 650 watts of peak pulse power. It utilizes a low loss internal input and output impedance matching structure to yield maximum device gain and to ease the implementation of external matching circuitry. The new generation bipolar transistor geometry utilizes a gold metallization system to achieve maximum reliability. Emitter ballast resistance is incorporated on the active cell for optimum thermal distribution and maximum reliability. All devices are 100% screened for large signal RF parameters.

Silicon Bipolar
- Ultra-high f_T

Class C Operation
- High Efficiency

Common Base Configuration
- Single Power Supply

Gold Metal
- Maximum Reliability

Emitter Ballasting
- Optimum Thermal Distribution

Internal Impedance Matching
- Ease of Use
- Ultra-low Loss Design

Be0 Package
- Unmatched Thermal Reliability

RF Test Fixture
- Broadband
- Matched to 50Ω
- Long-term Correlation
- 100% Device RF Screening
- No External Tuning Allowed
- Micro-strip structure on soft pc board with dielectric constant 10.2

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

Lot - SN	Freq (MHz)	Pin (W)	RL (dB)	Pout (W)	GP (dB)	dG (dB)	IC (A)	Nc (%)	Droop (dB)	VSWR-S 1.5:1 (P-F)	VSWR-LMT 3:1 (P-F)
	1450	88.0	-12.0	650	8.68		23.000	56.5	0.01	P	P
D3863-3	1500	87.0	-18.0	650	8.73	0.45	24.100	53.9	0.00	P	P
	1550	96.5	-18.0	650	8.28		25.300	51.4	-0.01	P	P

Vcc = 50V, 0.5μs ON 1.5μs off, repeated for 100μs, DF = 1%.

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MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Collector-Emitter Voltage	V_{CES}	--	75	V	--
BD	Emitter-Base Voltage	V_{EBO}	--	2	V	--
BD	Storage Temperature Range	T_{STG}	-60	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-60	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	0.07	°C/W	V_{CC} = 50V, 75µs – 1%, T_F = 25±5°C, Pin = 103W, Pout = 650W, N_C = 40%.
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071, Test Condition C
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Collector-Emitter Breakdown Voltage	BV_{CES}	75	--	V	I_C = 40mA, V_{BE} = 0V, T_F = 25±5°C.
100%	Zero Base Voltage Collector Leakage Current	I_{CES}	--	10	mA	V_{CE} = 50V, V_{BE} = 0V, T_F = 25±5°C.
100%	DC Current Gain	H_{FE}	20	150	--	V_{CE} = 5V, I_C = 500mA, T_F = 25±5°C.

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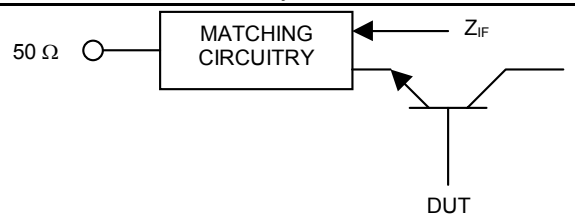
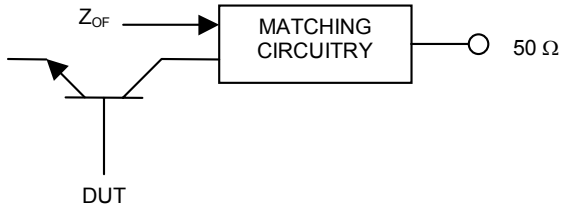
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	RL	-18	-10	dB	V_{CC}=50V, P_{OUT}=650W, Pulse = Note 2, T_F=30±5°C, F=F1
BD	Maximum Overdrive	$P_{IN(MAX)}$	--	137	W	V_{CC}=50V, P_{OUT}=650W, Pulse = Note 2, T_F=30±5°C, F=F1
100%	Power Gain	G_P	8.0	10.0	dB	V_{CC}=50V, P_{OUT}=650W, Pulse = Note 2, T_F=30±5°C, F=F1
100%	Input Power	Pin	65	103	W	V_{CC}=50V, P_{OUT}=650W, Pulse = Note 2, T_F=30±5°C, F=F1
100%	Collector Efficiency ($P_O/I_C/V_{CC}$)	N_C	40	75	%	V_{CC}=50V, P_{OUT}=650W, Pulse = Note 2, T_F=30±5°C, F=F1
BD	Pulse Amplitude Droop	Droop	-0.5	0.5	dB	V_{CC}=50V, P_{OUT}=650W, Pulse = Note 2, T_F=30±5°C, F=F1
BD	Second Harmonic Level	2F	-70	-20	dBc	V_{CC}=50V, P_{OUT}=650W, Pulse = Note 2, T_F=30±5°C, F=F1
100%	Stability into 1.5:1 VSWR	VSWR-S	--	1.5:1	--	V_{CC}=50V, P_{OUT}=650W, Pulse = Note 2, T_F=30±5°C, F=F1 Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse.
100%	Load Mismatch Tolerance	VSWR-LMT		3:1	--	V_{CC}=50V, P_{OUT}=650W, Pulse = Note 2, T_F=30±5°C, F=F1 Rotate 3:1 output VSWR through 360° phase. Survival.
BD	Pulse Risetime	RT	10	100	ns	V_{CC}=50V, P_{OUT}=650W, Pulse = Note 2, T_F=30±5°C, F=F1 Measure between 10% and 90% detected power points.

Note 1	F1 = 1450/1500/1550 MHz.
Note 2	Pulse Format : PW=0.5us ON, 1.5us OFF, repeated for 100us, DF=1%.
Note 3	T_F = Device flange temperature.
Note 4	Screen 'BD' = parameter qualified By Design.

RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (MHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
1450	1.73 –j3.25	1.10 –j1.15
1500	1.57 –j2.77	1.14 –j1.00
1550	1.45 –j2.37	1.18 –j0.90
Impedance Definition		

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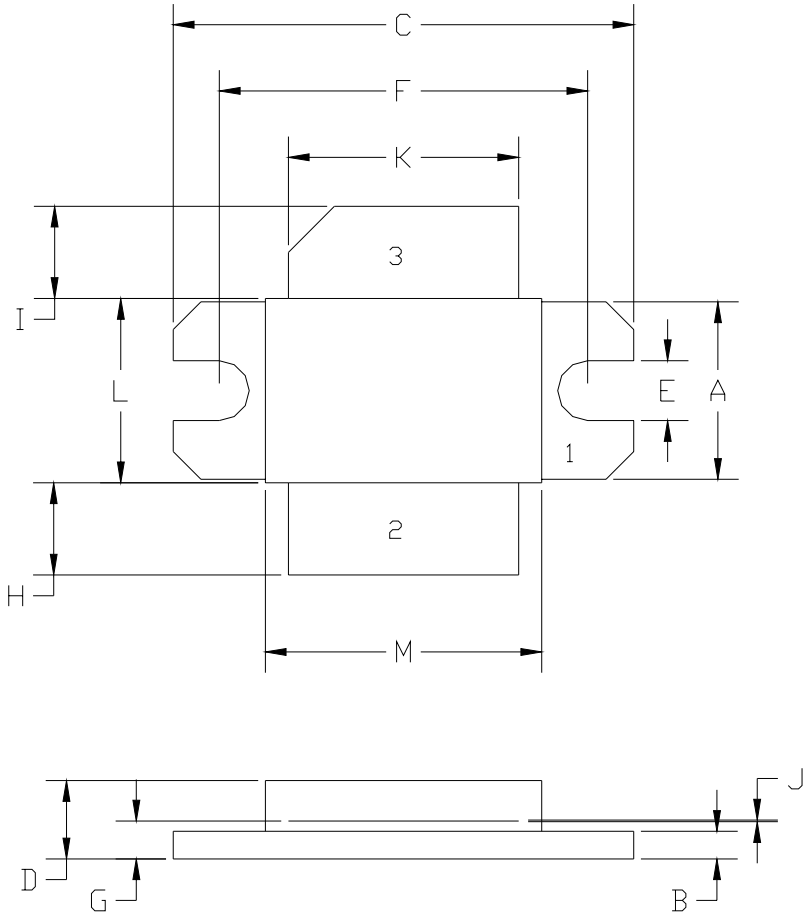
PACKAGE DIMENSIONAL OUTLINE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.380	0.390	9.65	9.91
B	0.043	0.053	--	--
C	0.905	1.005	22.99	25.53
D	0.178	0.188	4.52	4.78
E	0.125	0.135	3.18	3.43
F	0.795	0.805	20.19	20.45
G	0.082	0.092	2.08	2.34
H	0.185	0.215	4.70	5.46
I	0.185	0.215	4.70	5.46
J	0.002	0.004	0.05	0.10
K	0.495	0.505	12.57	12.83
L	0.395	0.405	10.03	10.29
M	0.595	0.605	15.11	15.37

PIN SCHEDULE	
1	BASE
2	EMITTER
3	COLLECTOR

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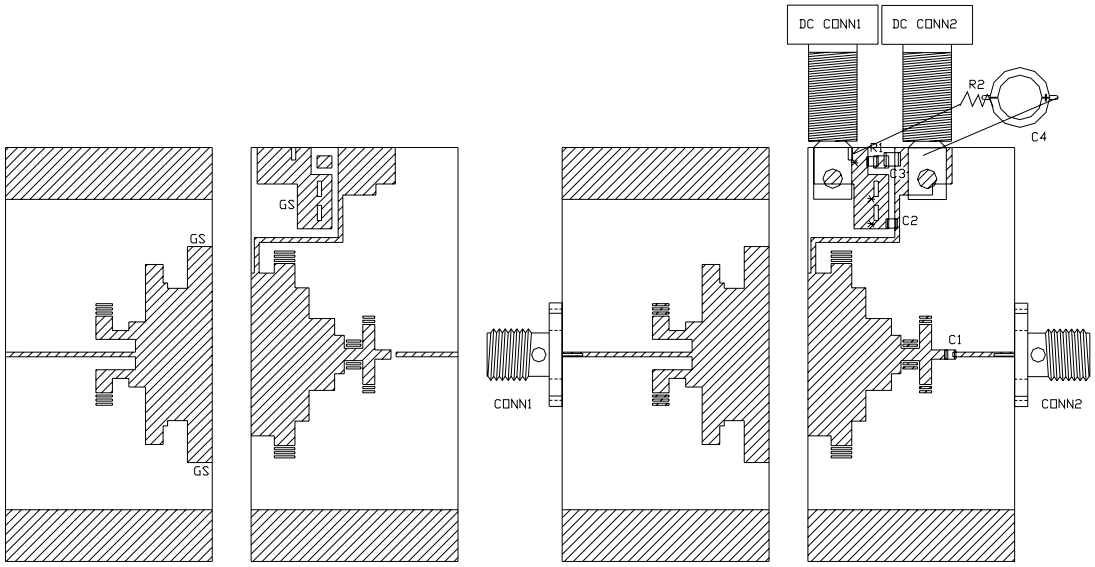

COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IB1416S650, MOUNT HARD TO THE RIGHT
PC BOARD	ROGERS #RO3010, TH=0.025" 1E/1E
C1	CHIP CAPACITOR, TYPE ATC100A, 82pF
C2	CHIP CAPACITOR, TYPE ATC100A, 100pF
C3	CHIP CAPACITOR, TYPE ATC100A, 2.2pF
C4	ELECTROLYTIC CAPACITOR, 68uF / 63V
C5 - NOT SHOWN	ELECTROLYTIC CAPACITOR, 2200uF / 63V
R1	CHIP RESISTOR, 10 ohms
R2	CHIP RESISTOR, 2 ohms
GS	GROUND SHIM, COPPER, TH=0.001"
CONN1, CONN2	SMA CONNECTOR, TYPE OS #2052-5636-02
INPUT PC BOARD CARRIER	2 INCH BRASS - 03
OUTPUT PC BOARD CARRIER	2 INCH BRASS - 03
TRANSISTOR CARRIER	2 INCH COPPER - 03
TRANSISTOR CLAMP	NORYL CLAMP -01
HEATSINK	2 INCH HEATSINK - 09
DC CONN1	BANANA JACK, BLACK
DC CONN2	BANANA JACK, RED
JP	JUMPER WIRE - 0.022" DIA TYPICAL
BLW	BIAS LINE WIRE - COPPER - 0.022" DIA TYPICAL
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

ASSEMBLY AND PARTS LIST

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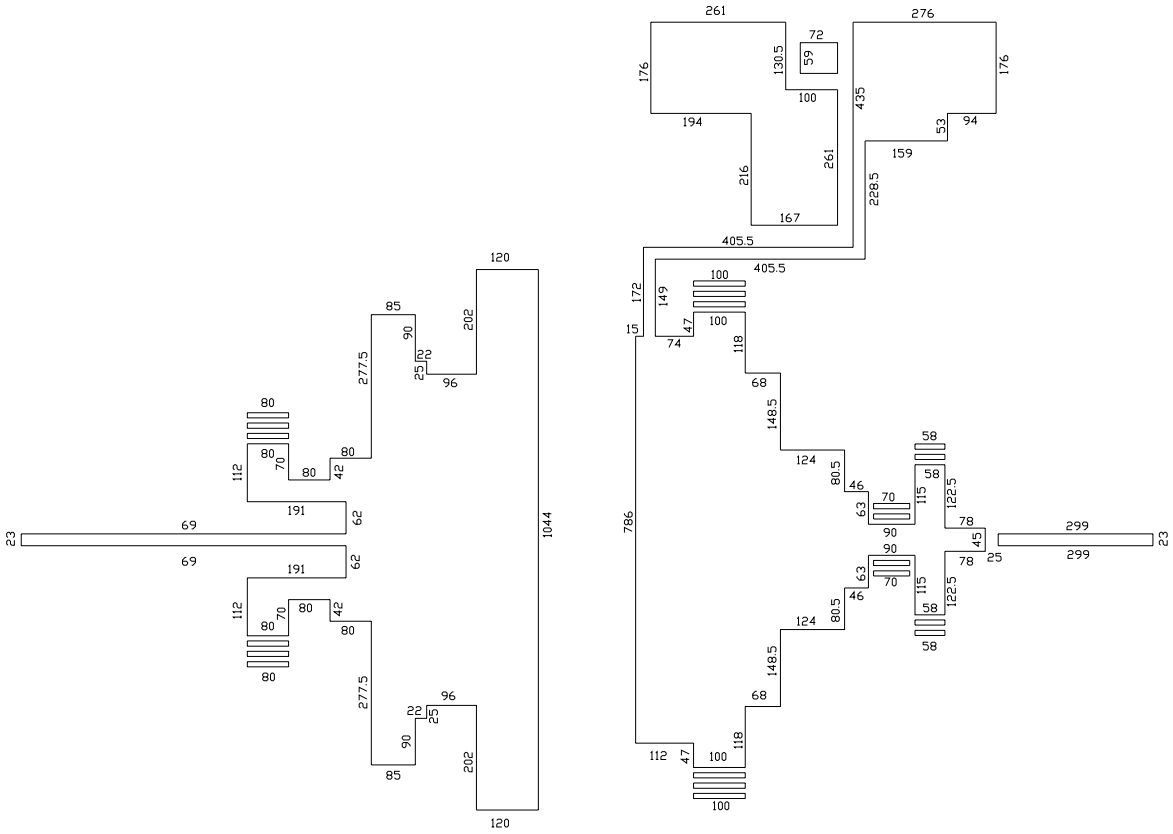

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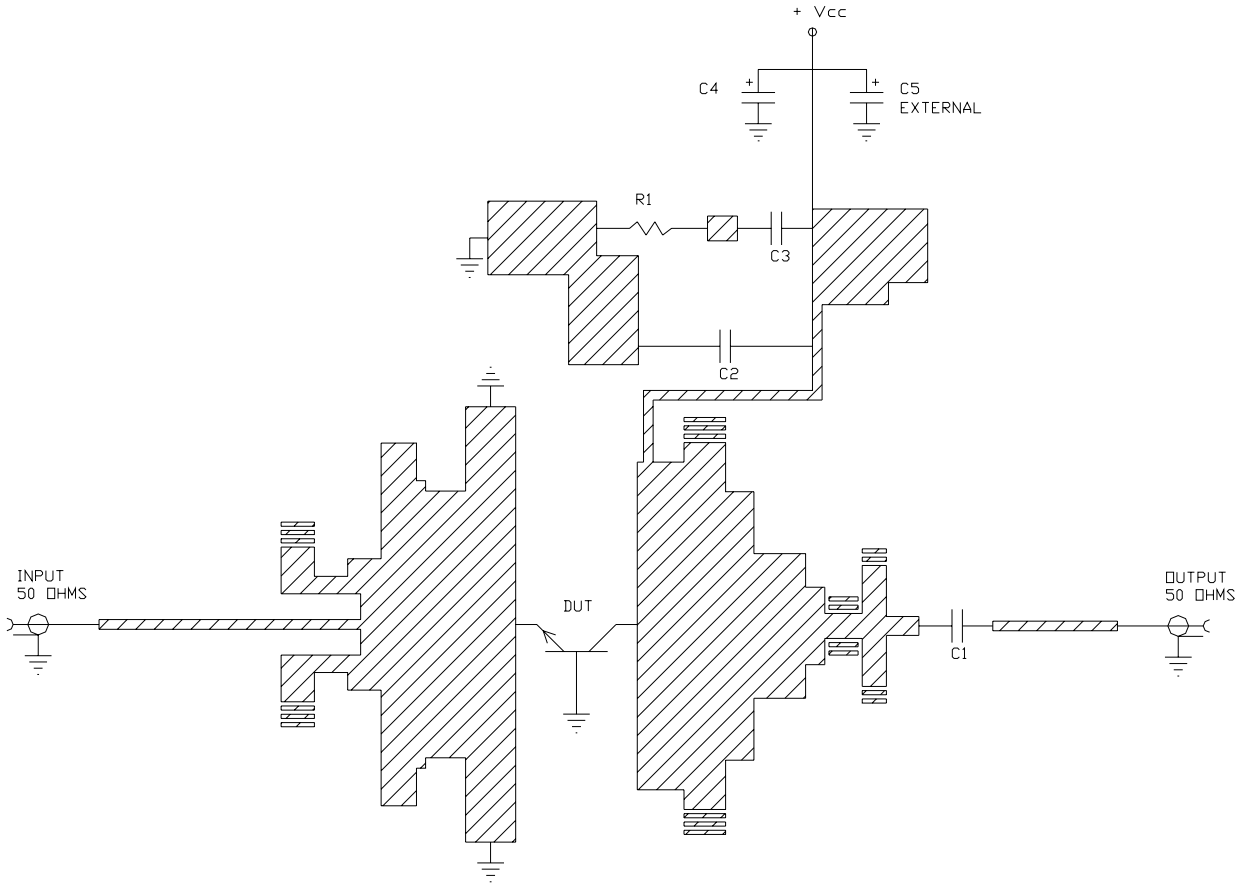

ELECTRICAL SCHEMATIC

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DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.

Maximum Ratings
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only and operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

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