4.25 Gbps, 3.3 V Low Noise, Transimpedance Amplifier

Data Sheet **ADN2882**

FEATURES

Bandwidth: 3.5 GHz
Input noise current density: 8 pA/√Hz
Optical sensitivity
–22.0 dBm[1]
–20.4 dBm[2]
Differential transimpedance: 3700 V/A
Power dissipation: 80 mW
Differential output swing: 260 mV p-p
Input overload current: 5.6 mA p-p
On-chip RSSI function
Low frequency cutoff: 12 kHz
On-chip PD filter: R_F = 200 Ω, C_F = 20 pF
Die size: 0.7 mm × 1.2 mm

APPLICATIONS

4.25 Gbps optical receivers
GbE/FC optical receivers
SFF-8472-compliant receivers
PIN/APD-TIA receiver optical subassemblies

GENERAL DESCRIPTION

The ADN2882 is a 3.3 V high gain SiGe transimpedance amplifier (TIA) which converts the small signal current of a photo detector to a large differential voltage output. The ADN2882 features a typical 475 nA input-referred noise, enabling an optical sensitivity of –22 dBm (0.85 A/W PIN). With a bandwidth of 3.5 GHz, the ADN2882 allows a data rate operation up to 4.25 Gbps. Typical power dissipation is 80 mW.

To facilitate the assembly in small form factor packages, such as TO-46 headers, the ADN2882 provides an on-chip RC filter (200 Ω, 20 pF) and features a 12 kHz low frequency cutoff without using an external capacitor. An on-chip RSSI circuit, which generates a voltage proportional to the average photodiode current, is available for power monitoring and assembly alignment.

The ADN2882 is available in die form. With a chip area of 1.2 mm × 0.7 mm, the TIA layout is optimized for TO-Can-based packages.

[1] Based on 1550 nm PIN, C_D = 0.5 ± 0.10 pF, responsivity = 0.85 A/W, ER = 9 dB, PRBS $2^{31} - 1$ at 4.25 Gbps, BER < 10^{-12}.
[2] Calculated result based on an 850 nm PIN, C_D = 0.5 ± 0.15 pF, responsivity = 0.48 A/W, ER = 9 dB, at 4.25 Gbps, BER < 10^{-12}.

FUNCTIONAL BLOCK DIAGRAM

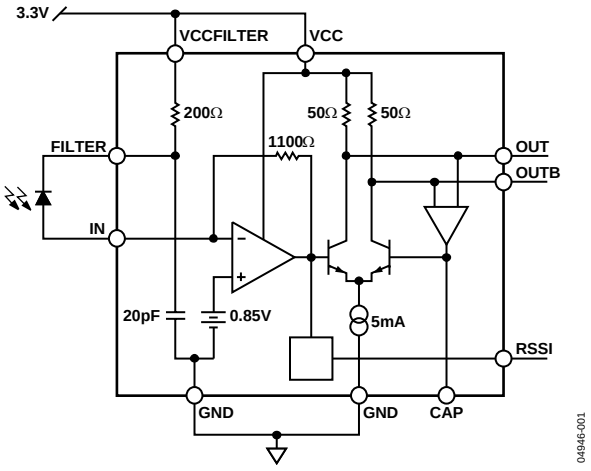

Figure 1.

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Technical Support **www.analog.com**

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REVISION HISTORY

9/14—Rev. 0 to Rev. A

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Changes to Figure 22 10
Changes to Ordering Guide 12

6/05—Revision 0: Initial Version

SPECIFICATIONS

Minimum/maximum VCC = 3.3 V ± 0.3 V, $T_{AMBIENT}$ = −40°C to +95°C; typical VCC = 3.3 V, $T_{AMBIENT}$ = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Bandwidth (BW)[1]	−3 dB	2.9	3.5		GHz
Total Input Referred RMS Noise (I_{RMS})	C_D = 0.5 pF, 4.0 GHz low-pass filter		475	605	nA
Small Signal Transimpedance (Z_T)[1]	100 MHz, differential	2800	3700	4800	V/A
	100 MHz, single-ended	1400	1850	2400	V/A
Low Frequency Cutoff	I_{IN} = 20 µA, CAP open		12		kHz
	I_{IN} = 500 µA, CAP open		84		kHz
Output Return Loss	DC to 4.0 GHz, differential		−25		dB
Input Overload Current	ER = 10 dB	3.5	5.6		mA p-p
Maximum Differential Output Swing	$I_{IN, P-P}$ = 2.0 mA	170	260	375	mV p-p
Output Data Transition Time	$I_{IN, P-P}$ = 1.0 mA; 20% to 80% rise/fall time		46		ps
PSRR	I_{IN} = 0 mA, 1 MHz < frequency <10 MHz		40		dB
Group Delay Variation	1.0 GHz to 4.0 GHz		±12		ps
Transimpedance Ripple	50 MHz to 1.0 GHz, single-ended		0.5		dB
Deterministic Jitter	10 µA < $I_{IN, P-P}$ ≤ 100 µA, K28.5 @ 4.25 Gbps		8		ps p-p
	100 µA < $I_{IN, P-P}$ ≤ 1.0 mA, K28.5 @ 4.25 Gbps		15		ps p-p
Linear Output Range	Differential output, <1 dB compression		190		mV p-p
Linear Input Current Range	Single-ended input, <1 dB compression		45		µA p-p
DC PERFORMANCE					
Power Dissipation	$I_{IN, AVE}$ = 0		80	110	mW
Input Voltage	Compliance voltage		0.85		V
Output Common-Mode Voltage	DC (50 Ω) terminated to VCC		VCC − 0.12		V
Output Impedance	Single-ended		50		Ω
PD Filter Resistance	R_F		200		Ω
PD Filter Capacitance	C_F		20		pF
RSSI Gain	$I_{IN, AVE}$ = 5 µA to 1 mA		0.83		V/mA
RSSI Offset	$I_{IN, AVE}$ = 10 µA		4.6		mV
RSSI Accuracy	5 µA < $I_{IN, P-P}$ ≤ 20 µA		±9		%
	20 µA < $I_{IN, P-P}$ ≤ 1 mA		±3		%

[1] A signal current equivalent to $I_{IN\,P-P}$ = 10 µA is applied to the TIA input. No input capacitor is applied.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VCC to GND)	5 V
Maximum Voltage to All Input and Output Signal Pins	VCC + 0.4 V
Minimum Voltage to All Input and Output Signal Pins	GND − 0.4 V
Maximum Input Current	10 mA
Storage Temperature Range	−65°C to +125°C
Operating Ambient Temperature Range	−40°C to +95°C
Maximum Junction Temperature	125°C
Die Attach Temperature (<30 sec)	410°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN LAYOUT AND FUNCTION DESCRIPTIONS

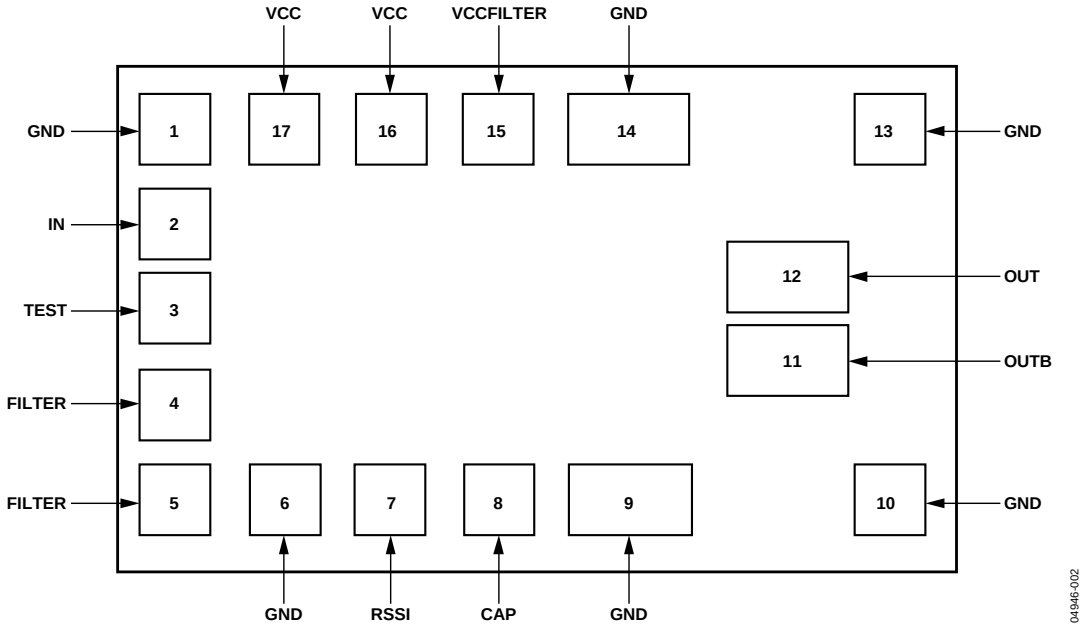

Figure 2. Pad Layout

Table 3. Pad Function Descriptions

Pad No.	Mnemonic	Pin Type[1]	Description
1	GND	P	Ground. (Input return.)
2	IN	AI	Current Input. Bond directly to a photodiode (PD) anode.
3	TEST	AI	Test Probe Pad. Do not connect.
4	FILTER	AO	Filter Output. Pad 4 and Pad 5 are metal connected. Optional bond to a PD cathode.
5	FILTER	AO	Filter Output. Pad 4 and Pad 5 are metal connected. Optional bond to a PD cathode.
6	GND	P	Ground.
7	RSSI	AO	Voltage Output. Provides average input current monitoring. Leave it open, if not used.
8	CAP	AI	Leave This Pin Open for Non-SONET Applications. For SONET applications, see Figure 10 and contact sales for assembly details.
9	GND	P	Ground. (Output return.)
10	GND	P	Ground. (Output return.)
11	OUTB	AO	Negative Output, CML, On-Chip 50 Ω Termination (AC or DC Termination).
12	OUT	AO	Positive Output, CML, On-Chip 50 Ω Termination (AC or DC Termination).
13	GND	P	Ground. (Output return.)
14	GND	P	Ground. (Output return.)
15	VCCFILTER	P	On-Chip Filter Supply. Connect to VCC to Enable On-Chip RC Filter (200 Ω, 20 pF). Leave it open, if not used.
16	VCC	P	3.3 V Power Supply. Place a 200 pF, RF decoupling capacitor close to the power pad to reduce the power noise.
17	VCC	P	3.3 V Power Supply. Place a 200 pF, RF decoupling capacitor close to the power pad to reduce the power noise.

[1] P = power; AI = analog input; and AO = analog output.

TYPICAL PERFORMANCE CHARACTERISTICS

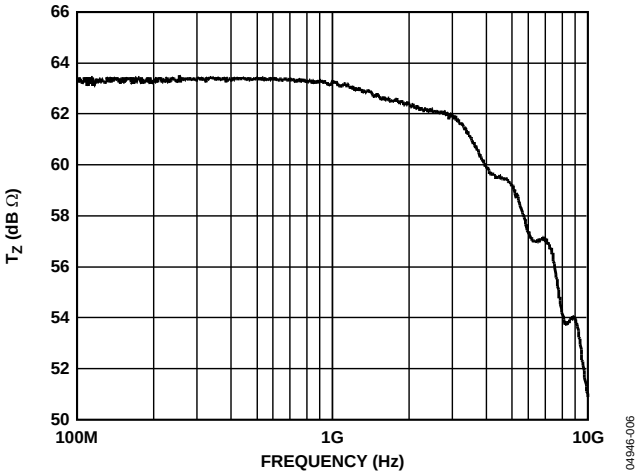

Figure 3. Single-Ended Transimpedance vs. Frequency

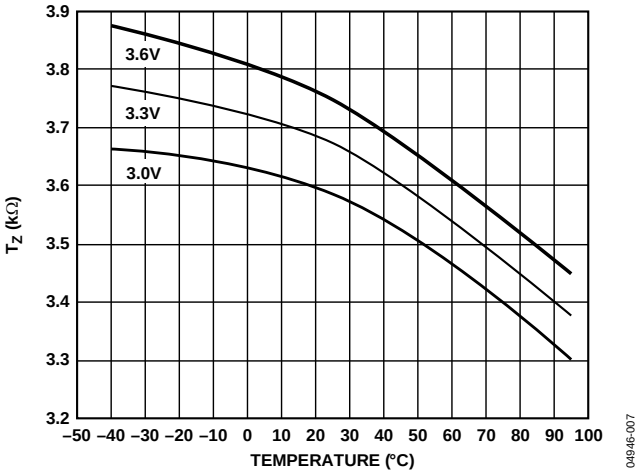

Figure 4. Differential Transimpedance vs. VCC and Temperature

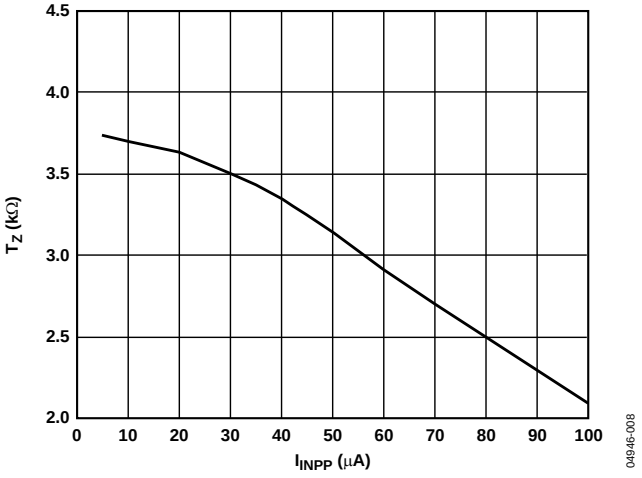

Figure 5. Differential Transimpedance vs. Input Current

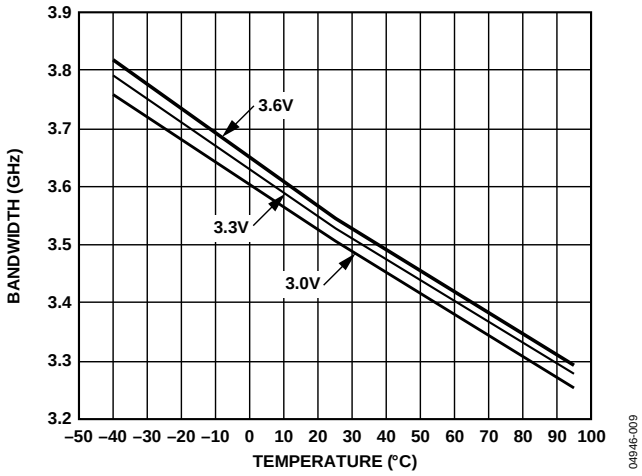

Figure 6. Bandwidth vs. VCC and Temperature

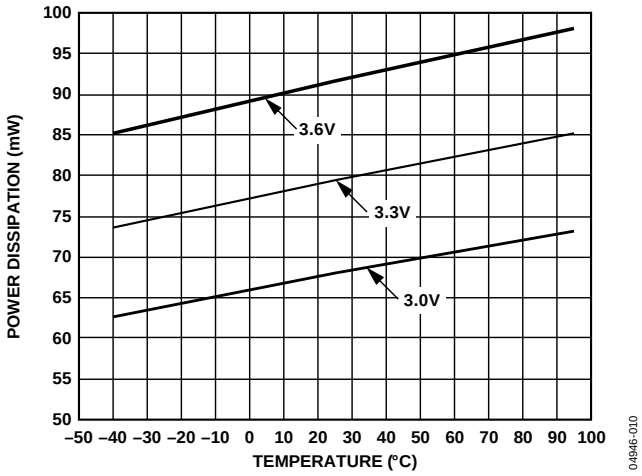

Figure 7. Power Dissipation vs. VCC and Temperature

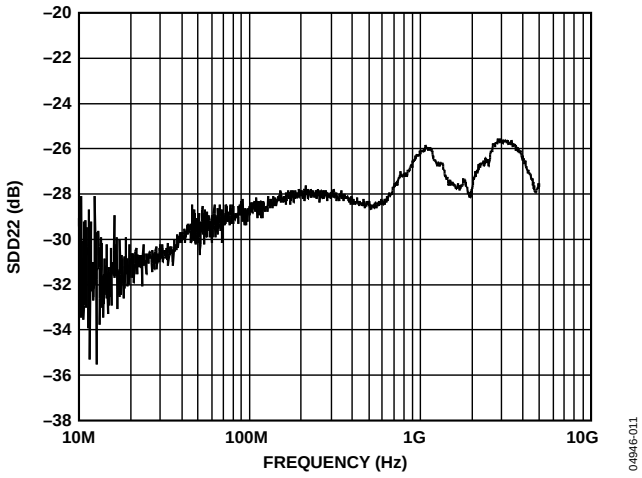

Figure 8. SDD22 vs. Frequency Up to 5 GHz, CAP = Open

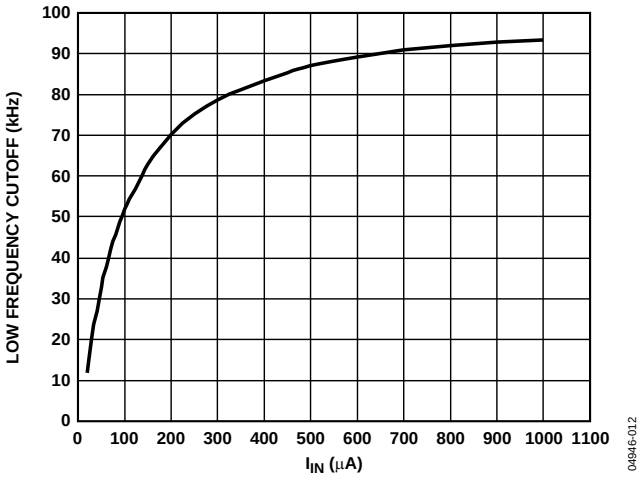

Figure 9. Low Frequency Cutoff vs. Input Current (CAP = OPEN)

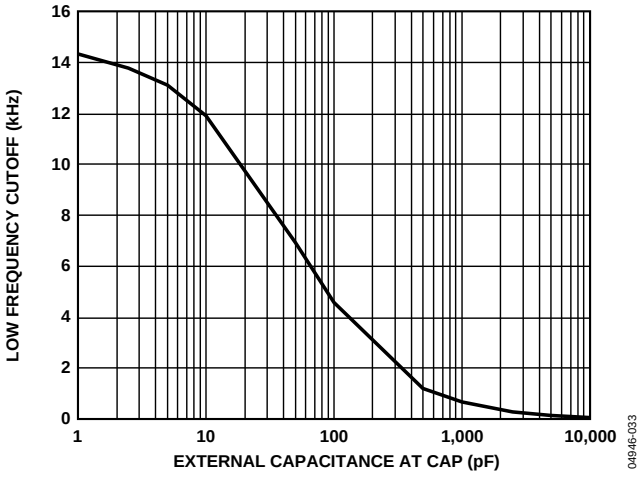

Figure 10. Low Frequency Cutoff vs. External Capacitance at CAP

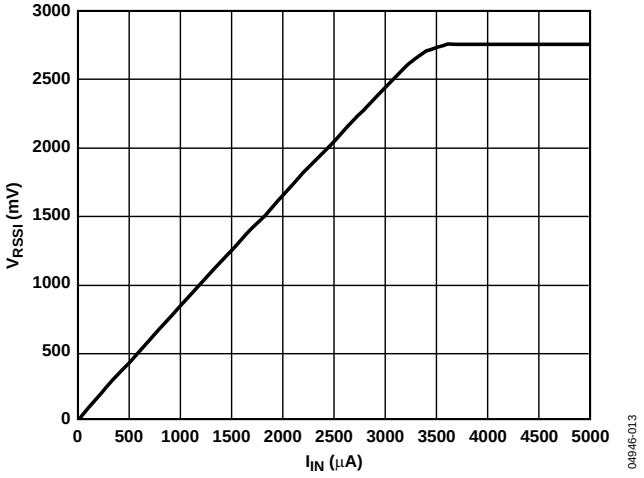

Figure 11. Full-Scale of RSSI Voltage Output vs. Input Current

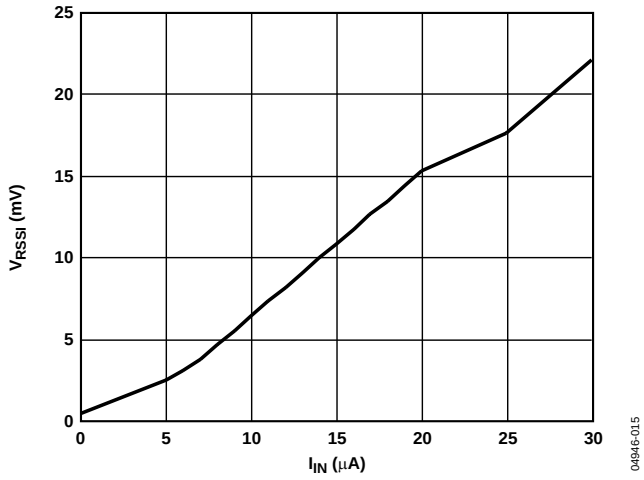

Figure 12. RSSI Voltage Output vs. Input Current (0 µA to 30 µA)

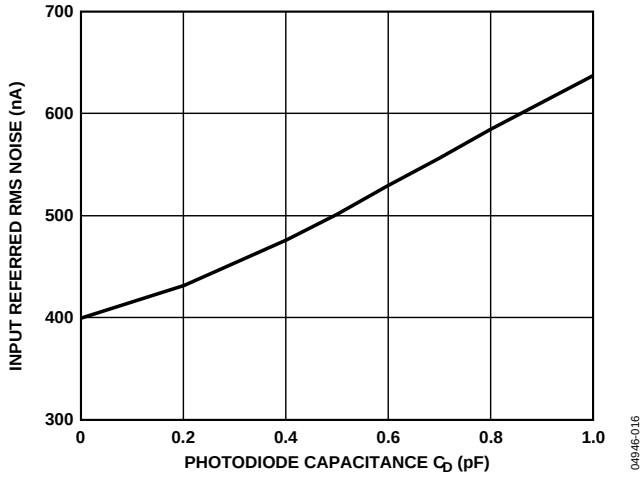

Figure 13. Input Referred Noise (DC to 4.0 GHz) vs. PD Capacitance

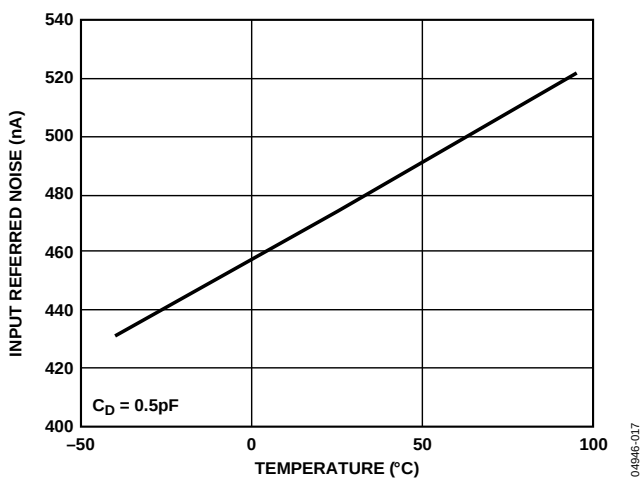

Figure 14. Input Referred Noise vs. Temperature

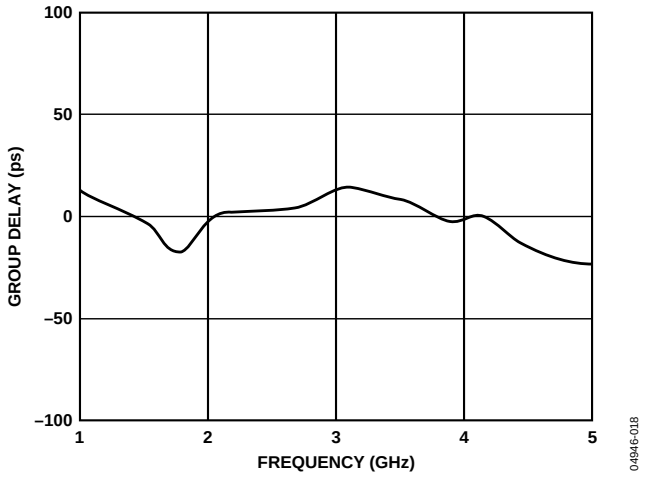

Figure 15. Group Delay vs. Frequency

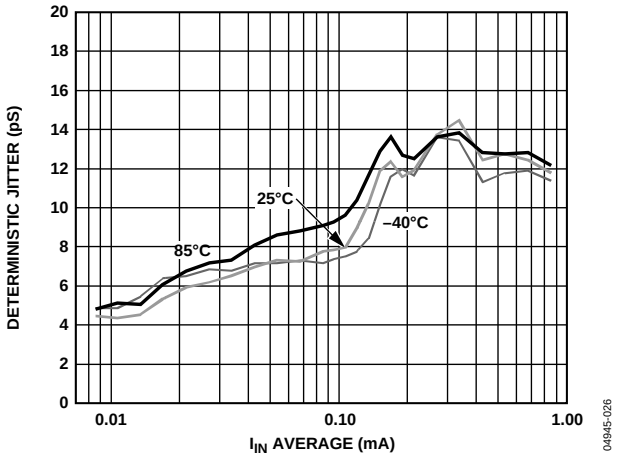

Figure 17. Deterministic Jitter vs. Input Current (K28.5 @ 4.25 Gbps)

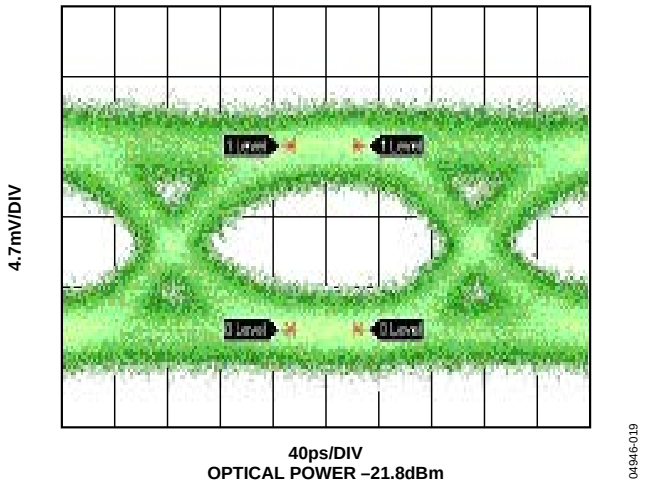

Figure 16. Output Eye at 4.25 Gbps
(1550 nm PD with Responsivity = 0.85 A/W,
ER = 9 dB, PRBS $2^{31} - 1$, BER < 10^{-12})

5-PIN TO-46 ASSEMBLY RECOMMENDATIONS

Contact sales for more details.

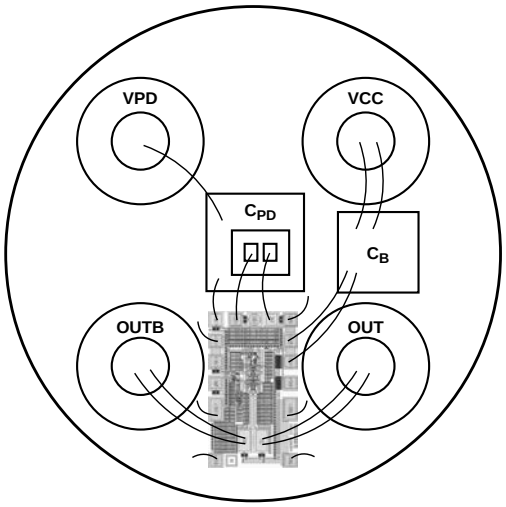

Figure 18. 5-Pin TO-46 with External Photodiode Supply VPD

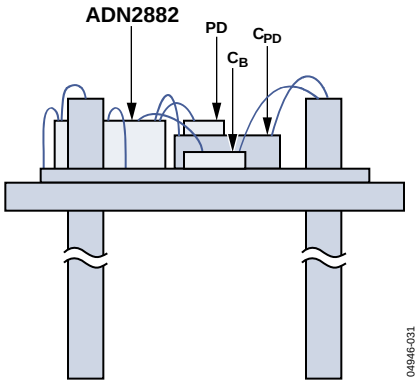

Figure 19. Side View of the Assembly

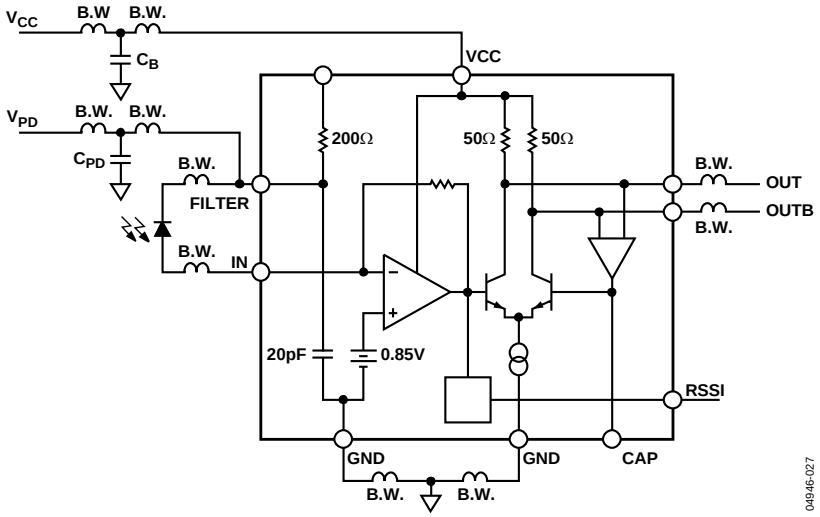

Figure 20. Equivalent Circuit of Assembly Including Bond Wires

Table 4. Bill of Materials (BOM)

Component	Description
PD	1× vendor specific, 4.25 Gbps, photodiode
TIA	1× ADN2882 (0.7 mm × 1.2 mm), 4.25 Gbps, transimpedance amplifier
C_B	1× 200 pF, RF single-layer capacitor
C_{PD}	1× 560 pF, RF single-layer capacitor

Notes

One mil thickness gold wire, ball bond recommended.

Minimize all GND bond-wire lengths.

Minimize IN, FILTER, OUT, and OUTB bond-wire lengths.

Maintain symmetry in length and orientation between OUT and OUTB bond wires.

Maintain symmetry between IN/FILTER and OUT/OUTB bond wires.

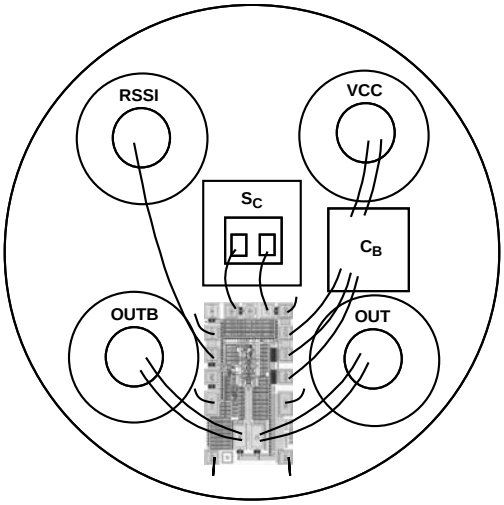

Figure 21. 5-Pin TO-46 with Internal PD Biasing and RSSI Output

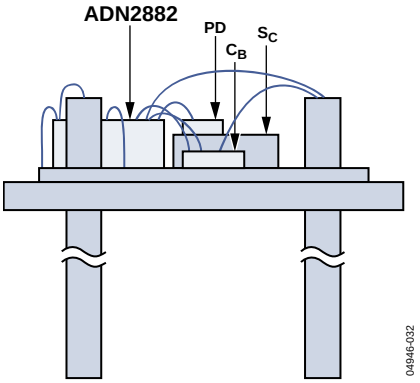

Figure 22. Side View of the Assembly

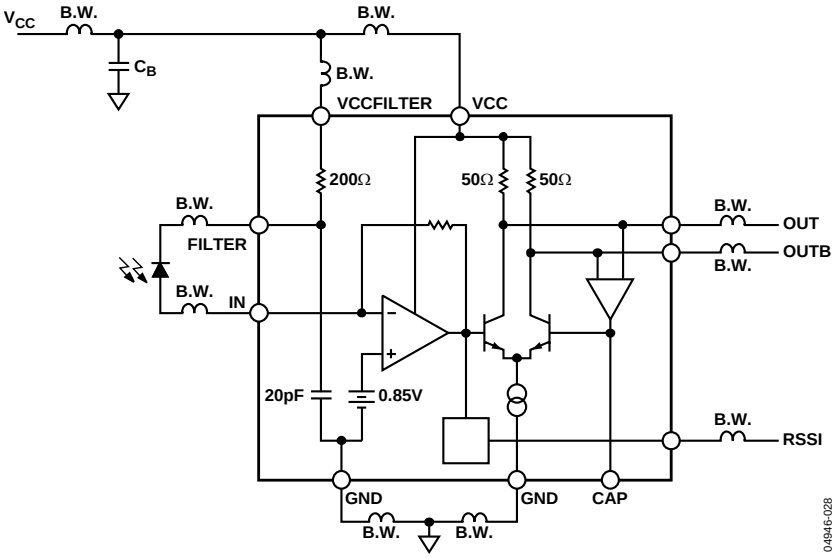

Figure 23. Equivalent Circuit of the Assembly Including Bond Wires

Table 5. Bill of Materials (BOM)

Component	Description
PD	1× vendor specific, 4.25 Gbps, photodiode
TIA	1× ADN2882 (0.7 mm × 1.2 mm), 4.25 Gbps, transimpedance amplifier
C_B	1× 200 pF, RF single-layer capacitor
S_C	1× ceramic standoff or 1× optional capacitor

Notes

One mil thickness gold wire, ball bond recommended.

Minimize all GND bond-wire lengths.

Minimize IN, FILTER, OUT, and OUTB bond-wire lengths.

Maintain symmetry in length and orientation between OUT and OUTB bond wires.

Maintain symmetry between IN/FILTER and OUT/OUTB bond wires.

4-PIN TO-46 ASSEMBLY RECOMMENDATIONS

Contact sales for more details.

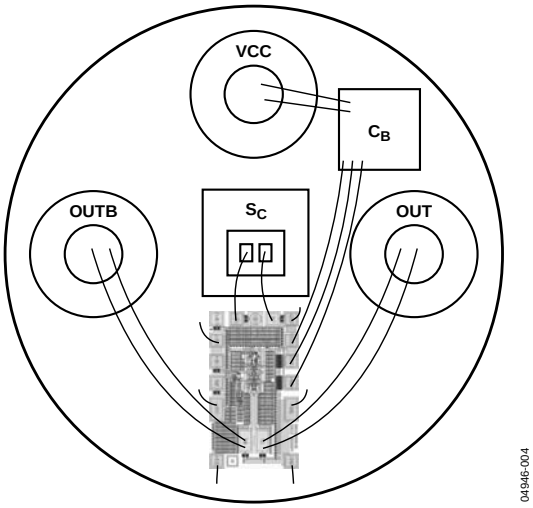

Figure 24. 4-Pin TO-46 with Internal PD Biasing

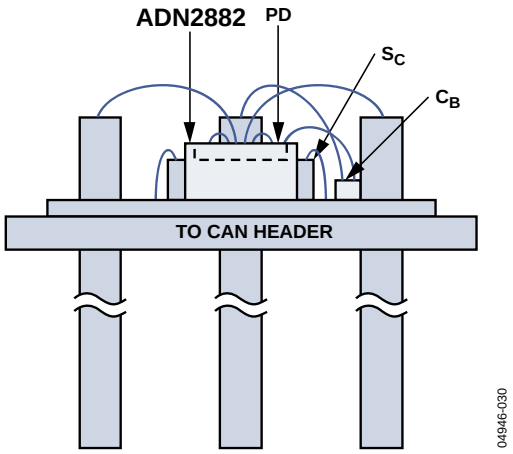

Figure 25. Side View of the Assembly

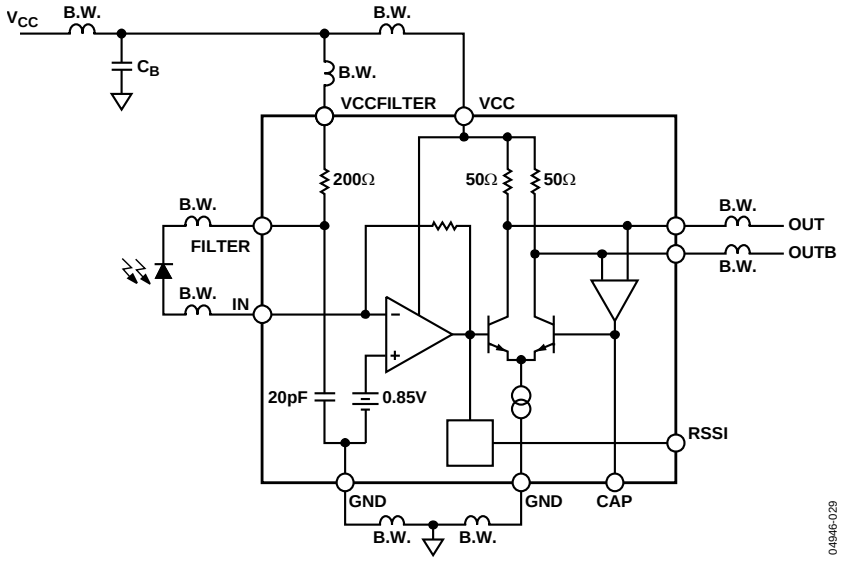

Figure 26. Equivalent Circuit of Assembly Including Bond Wires

Table 6. Bill of Materials (BOM)

Component	Description
PD	1× vendor specific, 4.25 Gbps, photodiode
TIA	1× ADN2882 (0.7 mm × 1.2 mm), 4.25 Gbps, transimpedance amplifier
C_B	1× 200 pF, RF single-layer capacitor
S_C	1× ceramic standoff or 1× optional capacitor

Notes

One mil thickness gold wire, ball bond recommended.

Minimize all GND bond-wire lengths.

Minimize IN, FILTER, OUT, and OUTB bond-wire lengths.

Maintain symmetry in length and orientation between OUT and OUTB bond wires.

Maintain symmetry between IN/FILTER and OUT/OUTB bond wires.

OUTLINE DIMENSIONS

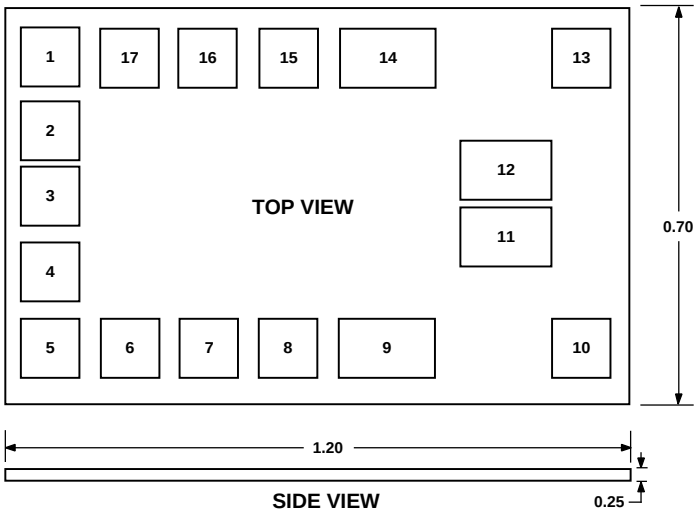

Figure 27. 17-Pad Bare Die Sales [CHIP]
C-17-1
Dimensions shown in millimeters

Table 7. Pad Coordinates

Pad No.	Mnemonic	X (µm)	Y (µm)
1	GND	−500	+260
2	IN	−500	+130
3	TEST	−500	+10
4	FILTER	−500	−120
5	FILTER	−500	−260
6	GND	−350	−260
7	RSSI	−200	−260
8	CAP	−50	−260
9	GND	+130	−260
10	GND	+500	−260
11	OUTB	+350	−60
12	OUT	+350	+60
13	GND	+500	+260
14	GND	+130	+260
15	VCCFILTER	−50	+260
16	VCC	−200	+260
17	VCC	−350	+260

DIE INFORMATION

Die Size

0.7 mm × 1.2 mm (edge to edge, including 1 mil scribe)

Die Thickness

10 mils = 0.25 mm

Passivation Openings

0.075 mm × 0.075 mm (Pad 1 to 8, 10, 13, and Pad 15 to 17)

0.144 mm × 0.075 mm (Pad 9, 11, 12, and Pad 14)

Passivation Composition

5000 Å Si3N4 (top)

5000 Å SiO2 (bottom)

Pad Composition

Al/1%Cu

Substrate Contact

To ground

ORDERING GUIDE

Model	Temperature	MOQ	Description[1]	Package Option
ADN2882ACHIPS	−40°C to +95°C	200	17-Pad Die Sales	C-17-1
ADN2882A-DF	−40°C to +95°C	5,704	Reconstituted die on 8" metal film frame	

[1] Contact Analog Devices, Inc., sales for more information on the film frame ADM2882A-DF.