19-2799; Rev 0; 4/03

可提供评估板

数字控制、可变增益的差分ADC驱动器/放大器

MAX2055

概述

MAX2055是高性能、数字控制、可变增益的差分模/数转换器(ADC)驱动器/放大器(DVGA)，针对30MHz至300MHz基站接收器应用而设计。

该器件集成了数字控制衰减器和高线性度单端到差分输出放大器，可以省去一个外部变压器，或是改善变压器耦合电路的偶次谐波失真，从而降低了对ADC前端抗混叠滤波器的要求。MAX2055设计用于ADC驱动，可动态调节增益或一次性设置通道增益，满足高性能设计的要求。衰减器提供精度为±0.2dB的23dB衰减范围。

MAX2055采用增强散热的20引脚TSSOP-EP封装，工作温度范围为-40°C至+85°C。

特性

- ♦ 30MHz至300MHz频率范围
- ♦ 单端到差分转换
- ♦ 可变增益范围为-3dB至+20dB
- ♦ 输出IP3为40dBm (70MHz，所有增益级)
- ♦ -76dBc二次谐波
- ♦ -69dBc三次谐波
- ♦ 噪声系数为5.8dB (最大增益)
- ♦ 数控增益的分辨率为1dB，精度为±0.2dB
- ♦ 可调偏置电流

应用

蜂窝基站

PHS/PAS基础架构

接收机增益控制

宽带系统

自动测试设备(ATE)

地面链路

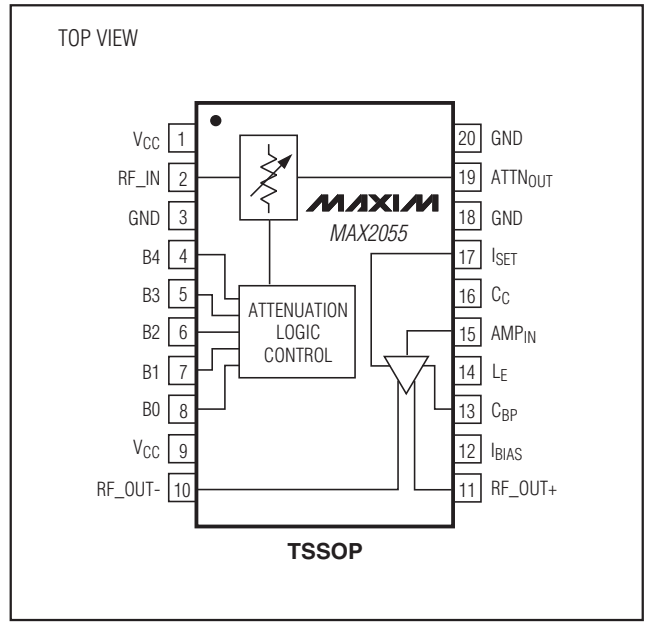
高性能ADC驱动器

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX2055EUP-T	-40°C to +85°C	20 TSSOP-EP*

**EP = 裸焊盘。*

引脚配置/功能框图



ABSOLUTE MAXIMUM RATINGS

All Pins to GND. .....-0.3V to +(V_{CC} + 0.25V)
Input Signal (RF_IN).....20dBm
Output Power (RF_OUT).....24dBm
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 21.7mW/°C above +70°C) 2.1W

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1; V_{CC} = +4.75V to +5.25V, GND = 0V. No input signals applied, and input and output ports are terminated with 50Ω. R1 = 1.13kΩ, T_A = -40°C to +85°C. Typical values are at V_{CC} = +5V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Supply Voltage	V_{CC}		4.75	5.0	5.25	V
Supply Current	I_{CC}			240	290	mA
I_{SET} Current	I_{SET}			1.1		mA
CONTROL INPUTS						
Control Bits		Parallel		5		Bits
Input Logic High			2			V
Input Logic Low					0.6	V
Input Leakage Current			-1.2		+1.2	µA

AC ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1; V_{CC} = +4.75V to +5.25V, GND = 0V, max gain (B0 = B1 = B2 = B3 = B4 = 0), R_1 = 1.13kΩ, P_{OUT} = 5dBm, f_{IN} = 70MHz, 50Ω system impedance. Typical values are at V_{CC} = +5V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	f_R		30		300	MHz
Gain	G			19.9		dB
Amplitude Unbalance		(Note 3)		0.06		dB
Phase Unbalance		(Note 3)		0.7		Degrees
Minimum Reverse Isolation				29		dB
Noise Figure	NF			5.8		dB
Output 1dB Compression Point	P_{1dB}			25.7		dBm
2nd-Order Output Intercept Point	OIP2	$f_1 + f_2$, f_1 = 70MHz, f_2 = 71MHz, 5dBm/tone at RF_OUT		75		dBm
3rd-Order Output Intercept Point	OIP3	All gain conditions, 5dBm/tone at RF_OUT		40		dBm
2nd Harmonic	$2f_{IN}$			-76		dBc
3rd Harmonic	$3f_{IN}$			-69		dBc
RF Gain-Control Range				23		dB
Gain-Control Resolution				1		dB
Attenuation Absolute Accuracy		Compared to the ideal expected attenuation		±0.2		dB
Attenuation Relative Accuracy		Between adjacent states		+0.05/ -0.2		dB
Gain Drift Over Temperature		T_A = -40°C to +85°C		±0.3		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1; V_{CC} = +4.75V to +5.25V, GND = 0V, max gain (B0 = B1 = B2 = B3 = B4 = 0), R_1 = 1.13kΩ, P_{OUT} = 5dBm, f_{IN} = 70MHz, 50Ω system impedance. Typical values are at V_{CC} = +5V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Flatness Over 50MHz Bandwidth		Peak-to-peak for all settings		0.5		dB
Attenuator Switching Time		50% control to 90% RF		40		ns
Input Return Loss		f_R = 30MHz to 300MHz, all gain conditions		15		dB
Output Return Loss		f_R = 30MHz to 250MHz, all gain conditions		15		dB
		f_R = 250MHz to 300MHz, all gain conditions		12		

Note 1: Guaranteed by design and characterization.

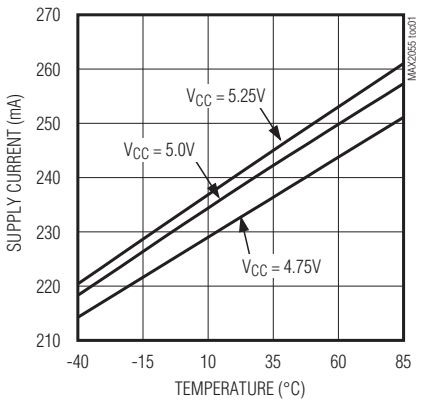
Note 2: All limits reflect losses of external components. Output measurements are taken at RF_OUT using the application circuit shown in Figure 1.

Note 3: The amplitude and phase unbalance are tested with 50Ω resistors connected from OUT+/OUT- to GND.

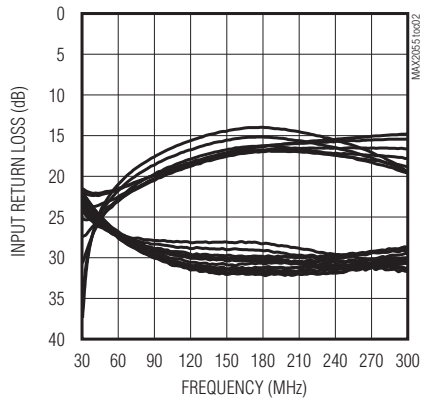
典型工作特性

(**Circuit of Figure 1**, V_{CC} = 5.0V, **R_1 = 1.13kΩ**, max gain (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

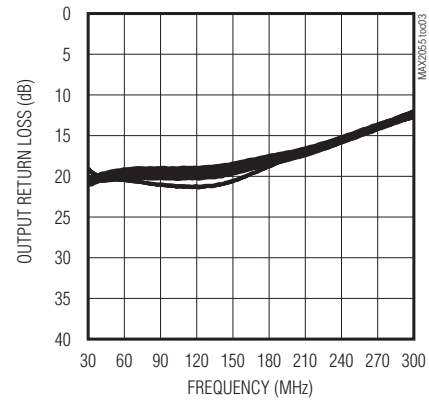
SUPPLY CURRENT vs. TEMPERATURE



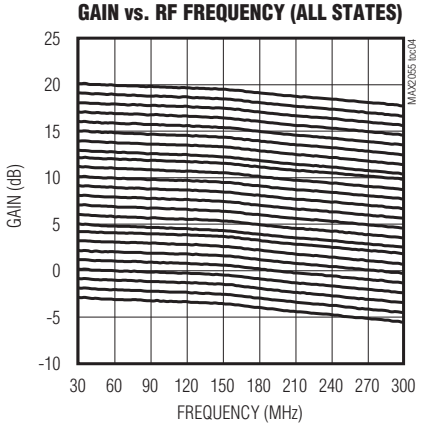
INPUT RETURN LOSS vs. RF FREQUENCY (ALL STATES)



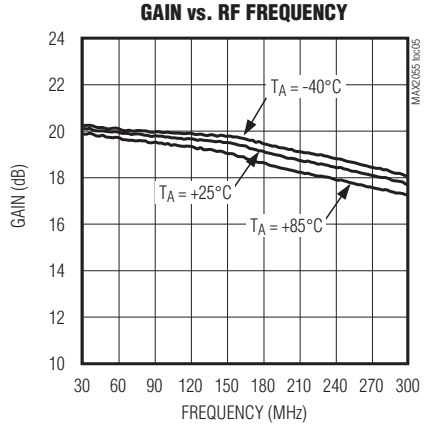
OUTPUT RETURN LOSS vs. RF FREQUENCY (ALL STATES)



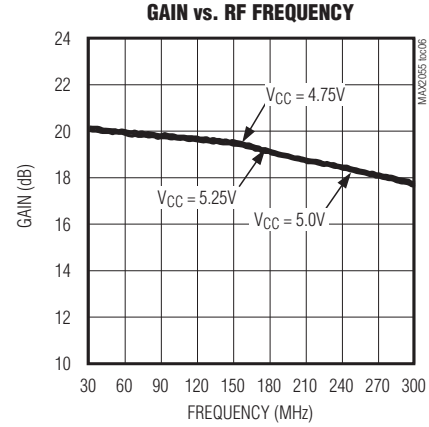
GAIN vs. RF FREQUENCY (ALL STATES)



GAIN vs. RF FREQUENCY



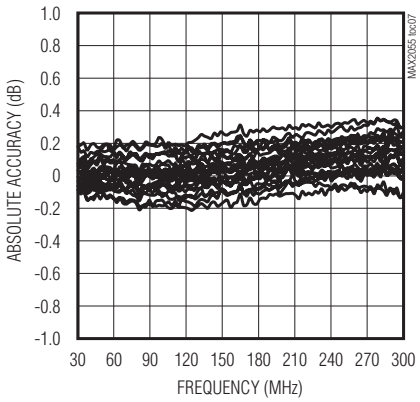
GAIN vs. RF FREQUENCY



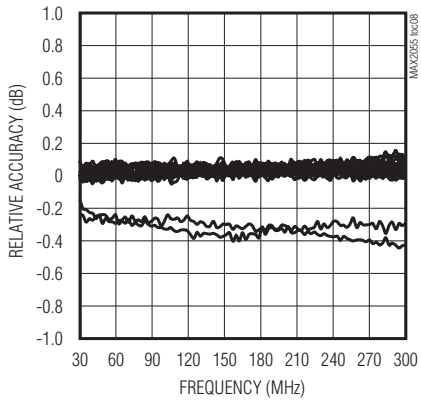
典型工作特性(续)

(**Circuit of Figure 1**, V_{CC} = 5.0V, **R_1 = 1.13kΩ**, max gain (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

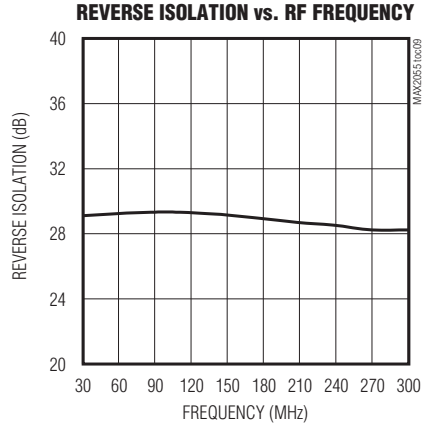
ATTENUATION ABSOLUTE ACCURACY (ALL STATES)



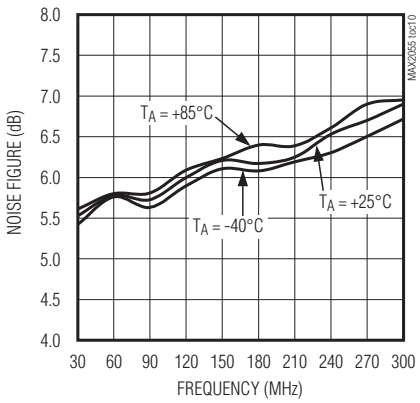
ATTENUATION RELATIVE ACCURACY (ALL STATES)



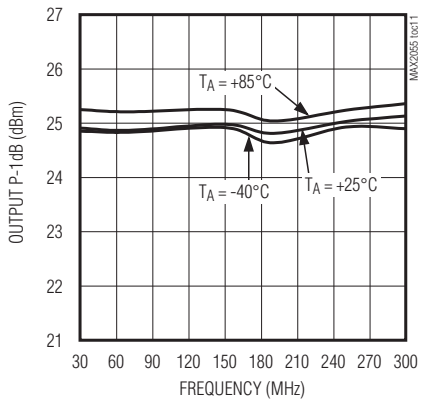
REVERSE ISOLATION vs. RF FREQUENCY



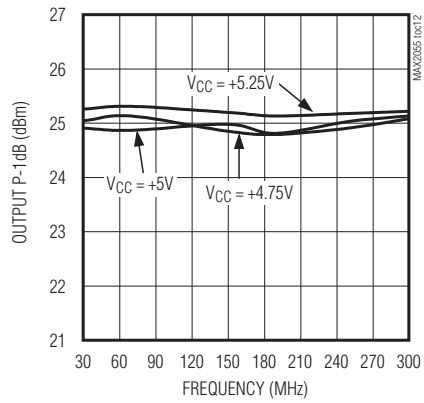
NOISE FIGURE vs. FREQUENCY



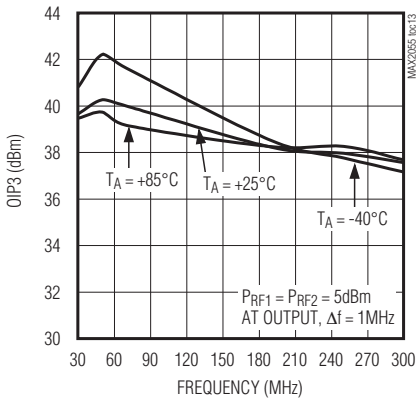
OUTPUT P-1dB vs. FREQUENCY



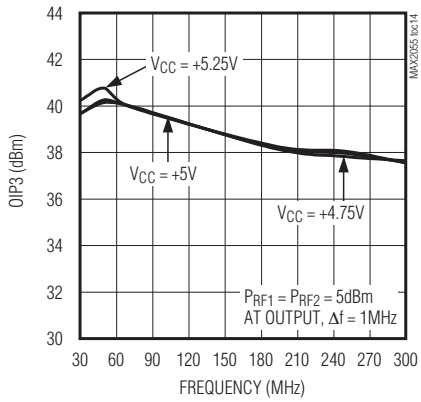
OUTPUT P-1dB vs. FREQUENCY



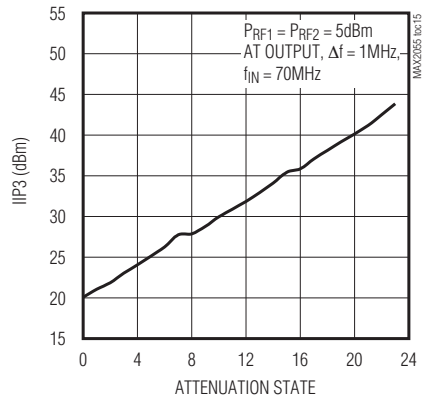
OUTPUT IP3 vs. FREQUENCY



OUTPUT IP3 vs. FREQUENCY



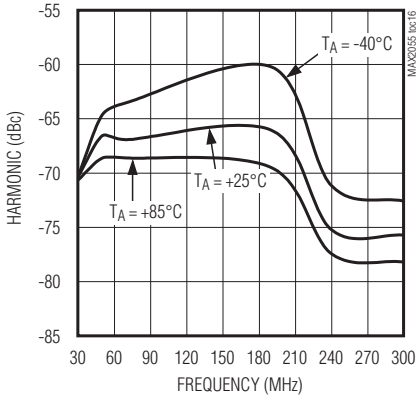
INPUT IP3 vs. ATTENUATION STATE



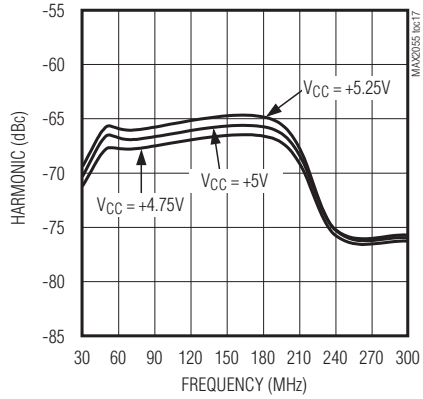
典型工作特性(续)

(**Circuit of Figure 1**, V_{CC} = 5.0V, **R_1 = 1.13kΩ**, max gain (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

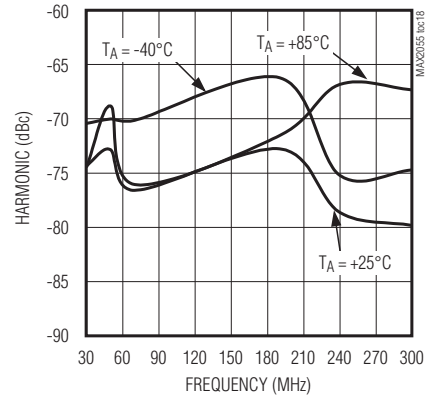
3RD HARMONIC vs. FREQUENCY



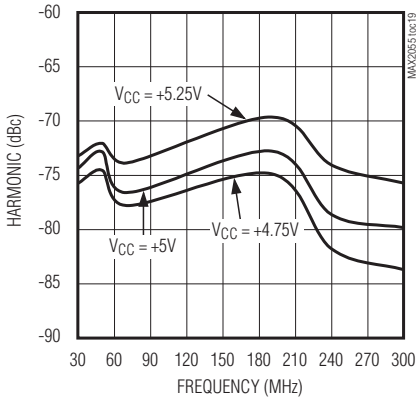
3RD HARMONIC vs. FREQUENCY



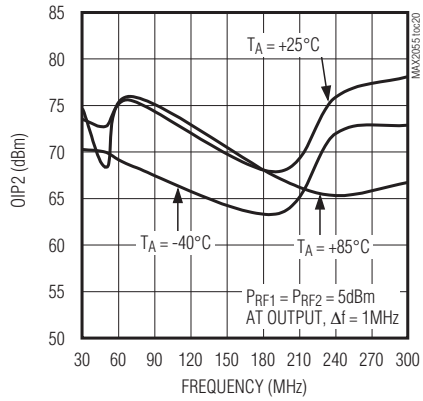
2ND HARMONIC vs. FREQUENCY



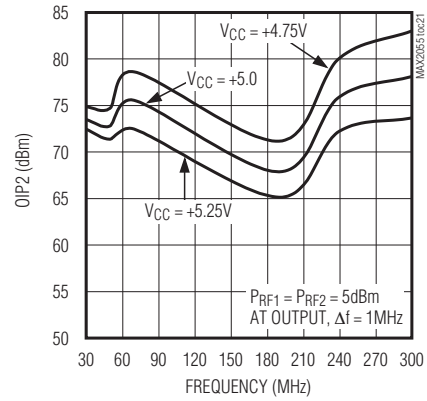
2ND HARMONIC vs. FREQUENCY



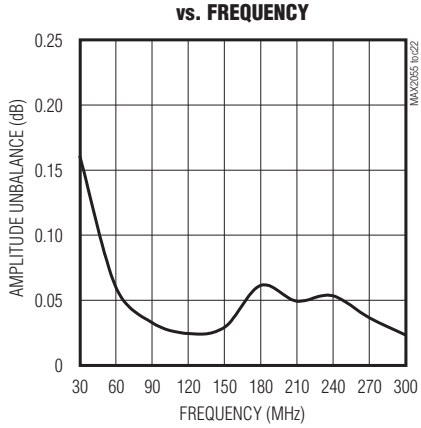
OUTPUT IP2 vs. FREQUENCY ($f_1 + f_2$)



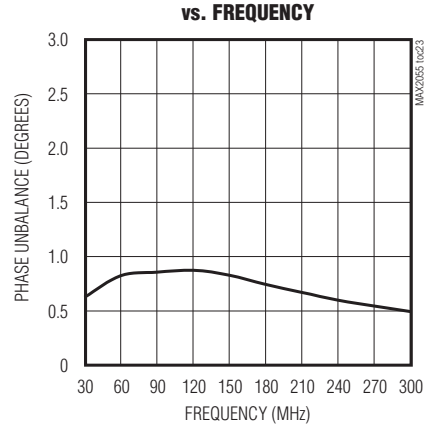
OUTPUT IP2 vs. FREQUENCY ($f_1 + f_2$)



OUTPUT-PORT AMPLITUDE UNBALANCE vs. FREQUENCY



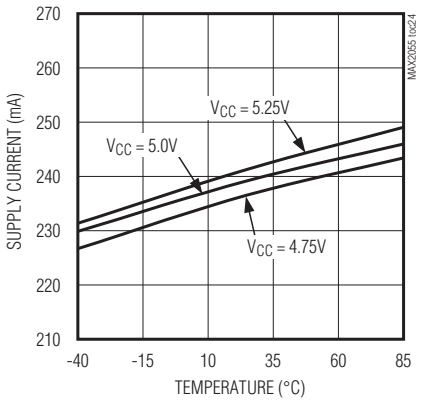
OUTPUT-PORT PHASE UNBALANCE vs. FREQUENCY



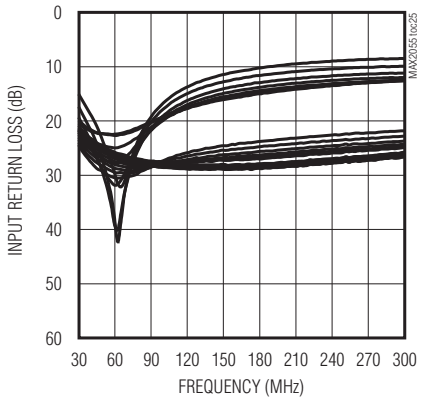
典型工作特性(续)

(**Circuit of Figure 2**, V_{CC} = 5.0V, **R_1 = 909Ω**, max gain, (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

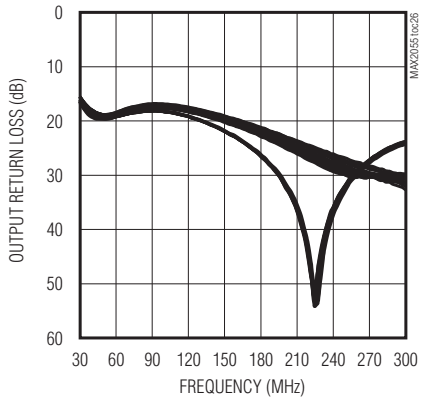
SUPPLY CURRENT vs. TEMPERATURE



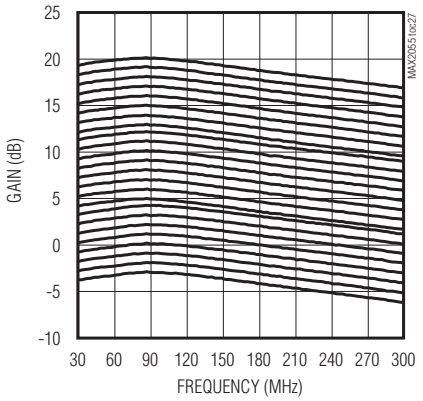
INPUT RETURN LOSS vs. RF FREQUENCY (ALL STATES)



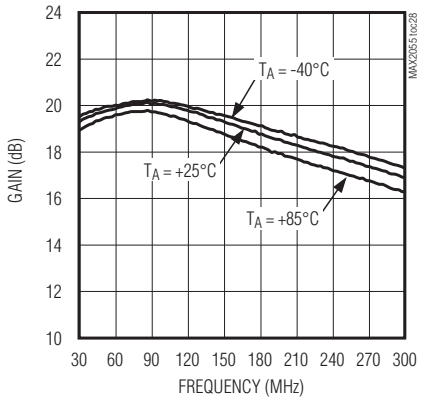
OUTPUT RETURN LOSS vs. FREQUENCY (ALL STATES)



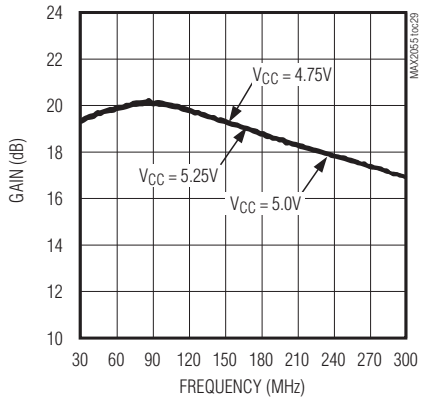
GAIN vs. RF FREQUENCY (ALL STATES)



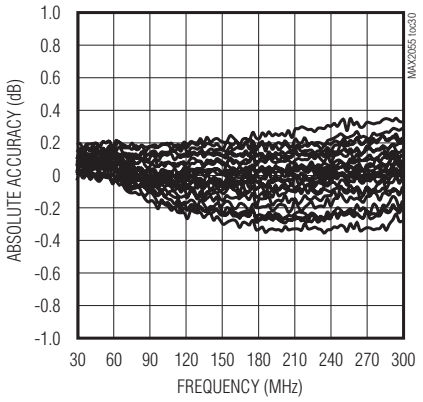
GAIN vs. RF FREQUENCY



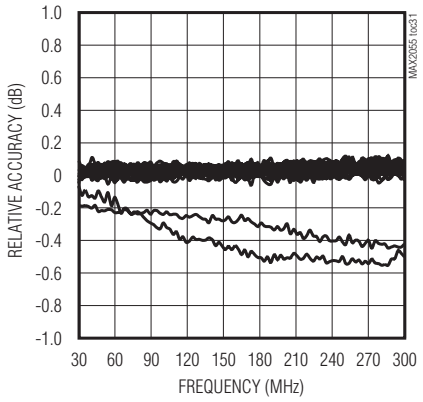
GAIN vs. RF FREQUENCY



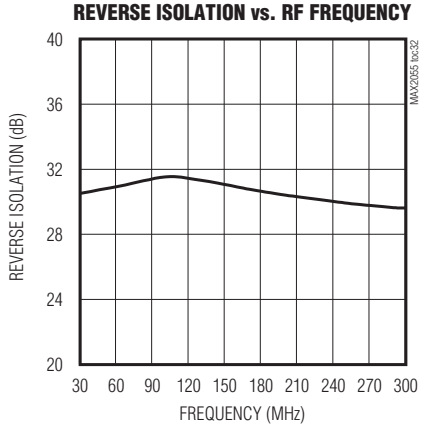
ATTENUATION ABSOLUTE ACCURACY (ALL STATES)



ATTENUATION RELATIVE ACCURACY (ALL STATES)



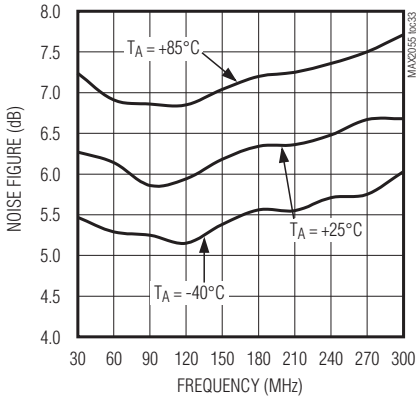
REVERSE ISOLATION vs. RF FREQUENCY



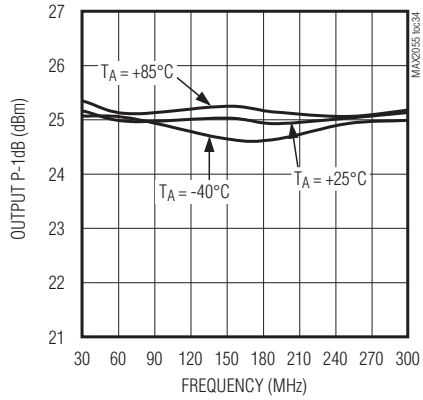
典型工作特性(续)

(**Circuit of Figure 2**, V_{CC} = 5.0V, **R_1 = 909Ω**, max gain, (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

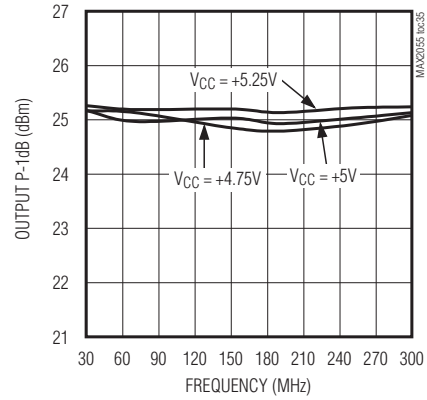
NOISE FIGURE vs. FREQUENCY



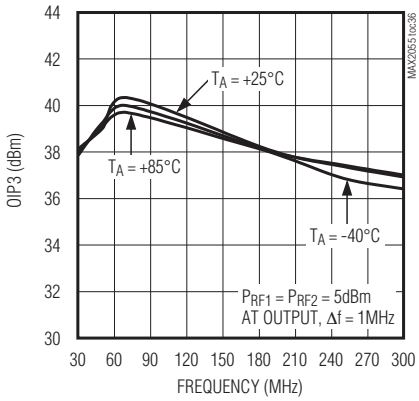
OUTPUT P-1dB vs. FREQUENCY



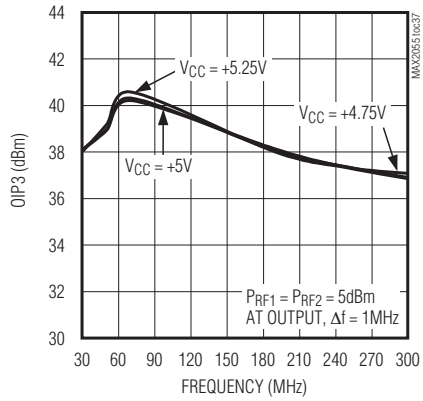
OUTPUT P-1dB vs. FREQUENCY



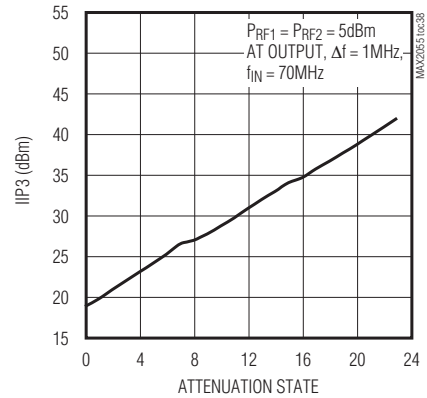
OUTPUT IP3 vs. FREQUENCY



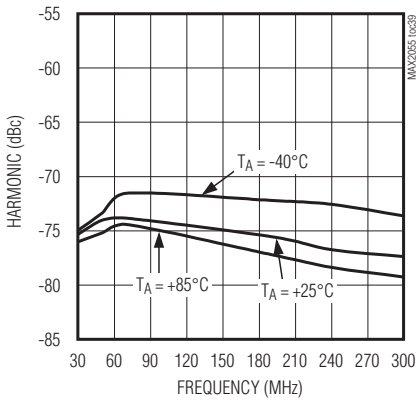
OUTPUT IP3 vs. FREQUENCY



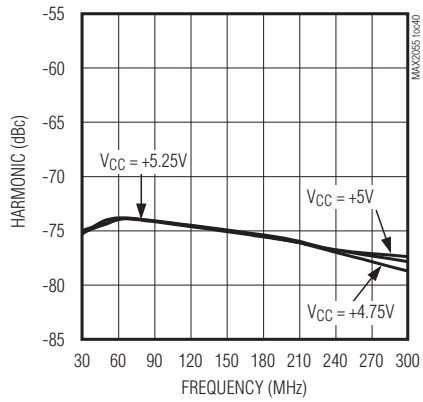
INPUT IP3 vs. ATTENUATION STATE



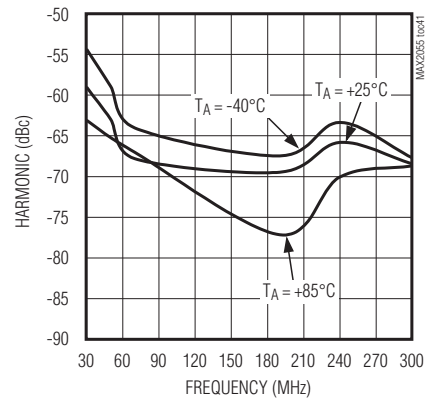
3RD HARMONIC vs. FREQUENCY



3RD HARMONIC vs. FREQUENCY



2ND HARMONIC vs. FREQUENCY

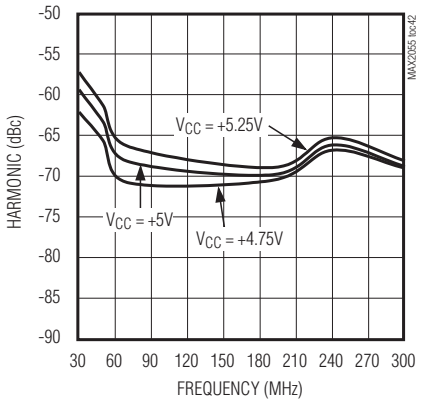


数字控制、可变增益的差分ADC驱动器/放大器

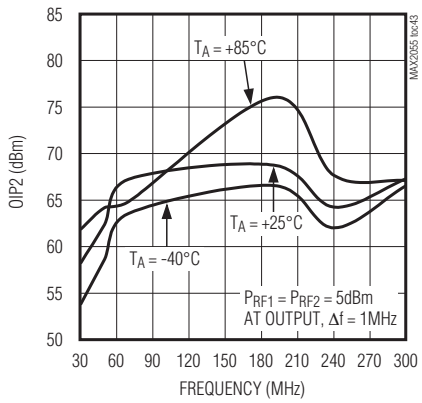
典型工作特性(续)

(**Circuit of Figure 2**, V_{CC} = 5.0V, **R_1 = 909Ω**, max gain, (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

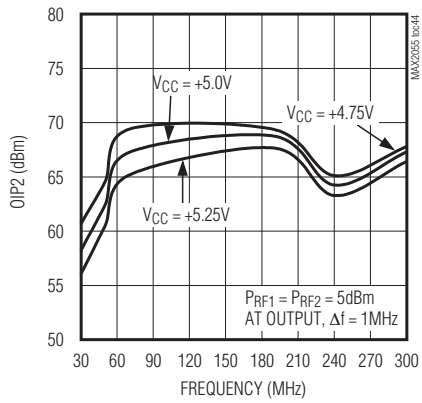
2ND HARMONIC vs. FREQUENCY



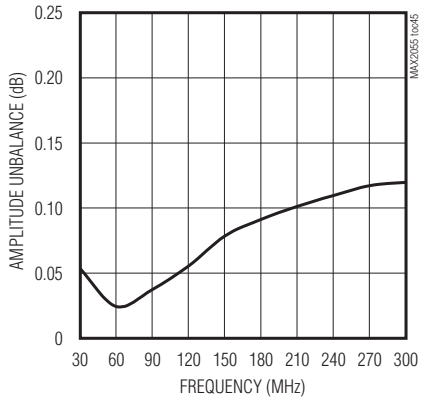
OUTPUT IP2 vs. FREQUENCY ($f_1 + f_2$)



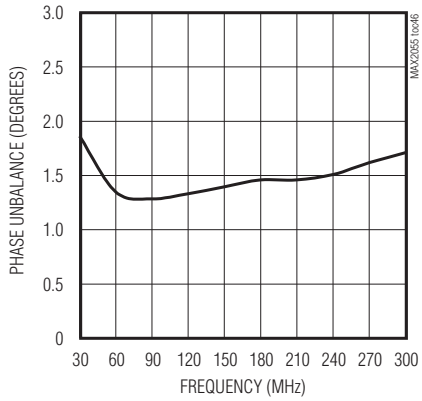
OUTPUT IP2 vs. FREQUENCY ($f_1 + f_2$)



OUTPUT-PORT AMPLITUDE UNBALANCE vs. FREQUENCY



OUTPUT-PORT PHASE UNBALANCE vs. FREQUENCY



引脚说明

引脚	名称	功能
1, 9	V_{CC}	电源，在尽可能靠近该引脚的位置用电容将其旁路至GND，如典型应用电路所示(图1和图2)。
2	RF_IN	信号输入，在整个工作频率范围内，内部匹配到50Ω。推荐元件请参考典型应用电路。
3, 18, 20, EP	GND	地，在PCB上采用低寄生电感布板技术，将裸焊盘焊接到电路板的地层。
4–8	B4–B0	衰减控制位，数字输入用于衰减控制，衰减设置请参考表3。
10	RF_OUT-	反相差分信号输出。需要外部扼流电感(典型电流为120mA)配合隔直流电容上拉至V_{CC}；参见图1和图2。
11	RF_OUT+	同相差分信号输出。需要外部扼流电感(典型电流为120mA)配合隔直流电容上拉至V_{CC}；参见图1和图2。
12	I_{BIAS}	放大器偏置输入，详细的连接方式参见图1和图2。
13	C_{BP}	旁路电容，详细的连接方式参见图1和图2。
14	L_E	放大器直流地，需要一个扼流电感处理电源电流。电感的直流电阻应小于0.2Ω。
15	AMP_{IN}	放大器输入，需要直流耦合以提供偏置。
16	C_C	补偿电容，为保证器件的稳定性，需连接至AMP_{IN} (第15引脚)。
17	I_{SET}	在I_{SET}和GND之间连接R1 (具体数值请参考表1或表2)。
19	$ATTN_{OUT}$	衰减器输出，需要外部隔直流电容。

表1. 图1电路的推荐元件

COMPONENT	VALUE	SIZE
C1, C3–C6, C8, C9, C10, C12	1nF	0603
C2, C11	100pF	0603
L1, L3	330nH	0603
L2	100nH	0603
L4, L5	680nH	1008
R1	1.13kΩ	0603
R7	10Ω	0603
T1, T2	1:1	—

表2. 图2电路的推荐元件

COMPONENT	VALUE	SIZE
C1, C3, C4, C5, C7–C10, C12	1nF	0603
C2, C11	100pF	0603
L1, L2, L3	330nH	0603
L4, L5	680nH	1008
R1	909Ω	0603
R7	10Ω	0603
T2	1:1	—

数字控制、可变增益的差分ADC驱动器/放大器

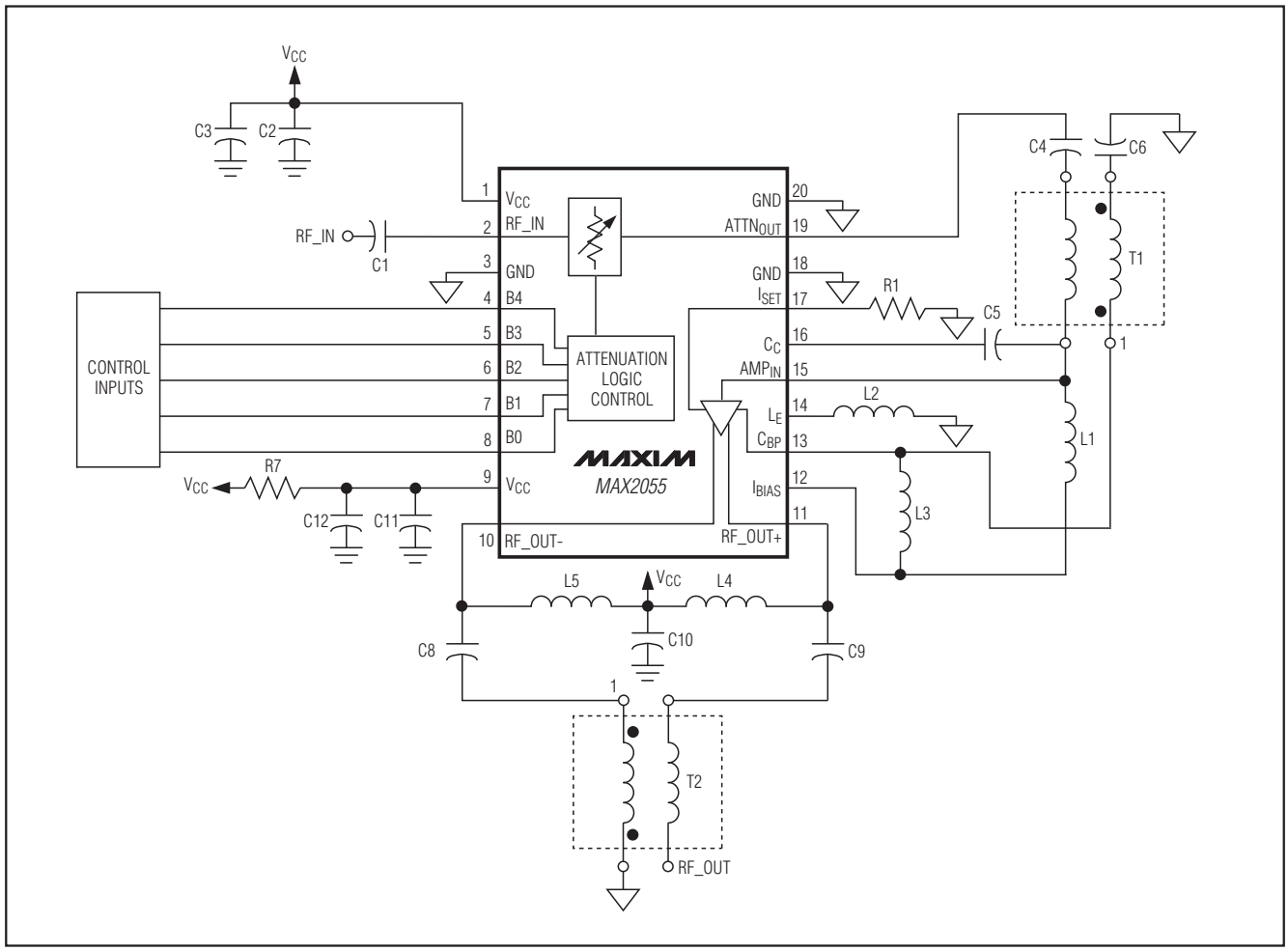


图1. 典型应用电路

详细说明

MAX2055是宽动态范围、数字控制的可变增益、差分模/数转换器(ADC)驱动器/放大器(DVGA)，针对30MHz至300MHz应用设计。该放大器适用于50Ω单端输入和50Ω差分输出系统。

MAX2055集成了具有23dB可选衰减范围的数字衰减器和高线性度单端至差分输出放大器。衰减器的数字控制功能通过5条逻辑控制线(B0–B4)实现。片上衰减器可提供高达23dB的衰减，精度为±0.2dB。这款单端输入至差分输出的放大器利用负反馈技术在整个带宽内实现高增益和高线性度。

应用信息

数字控制衰减器

该数字衰减器通过5条逻辑线：B0、B1、B2、B3和B4控制，表3列出了衰减设置。衰减器的输入和输出需要外部隔直流电容。当控制位设置为0dB (B0 = B1 = B2 = B3 = B4 = 0)时，衰减器的插入损耗约为2dB。

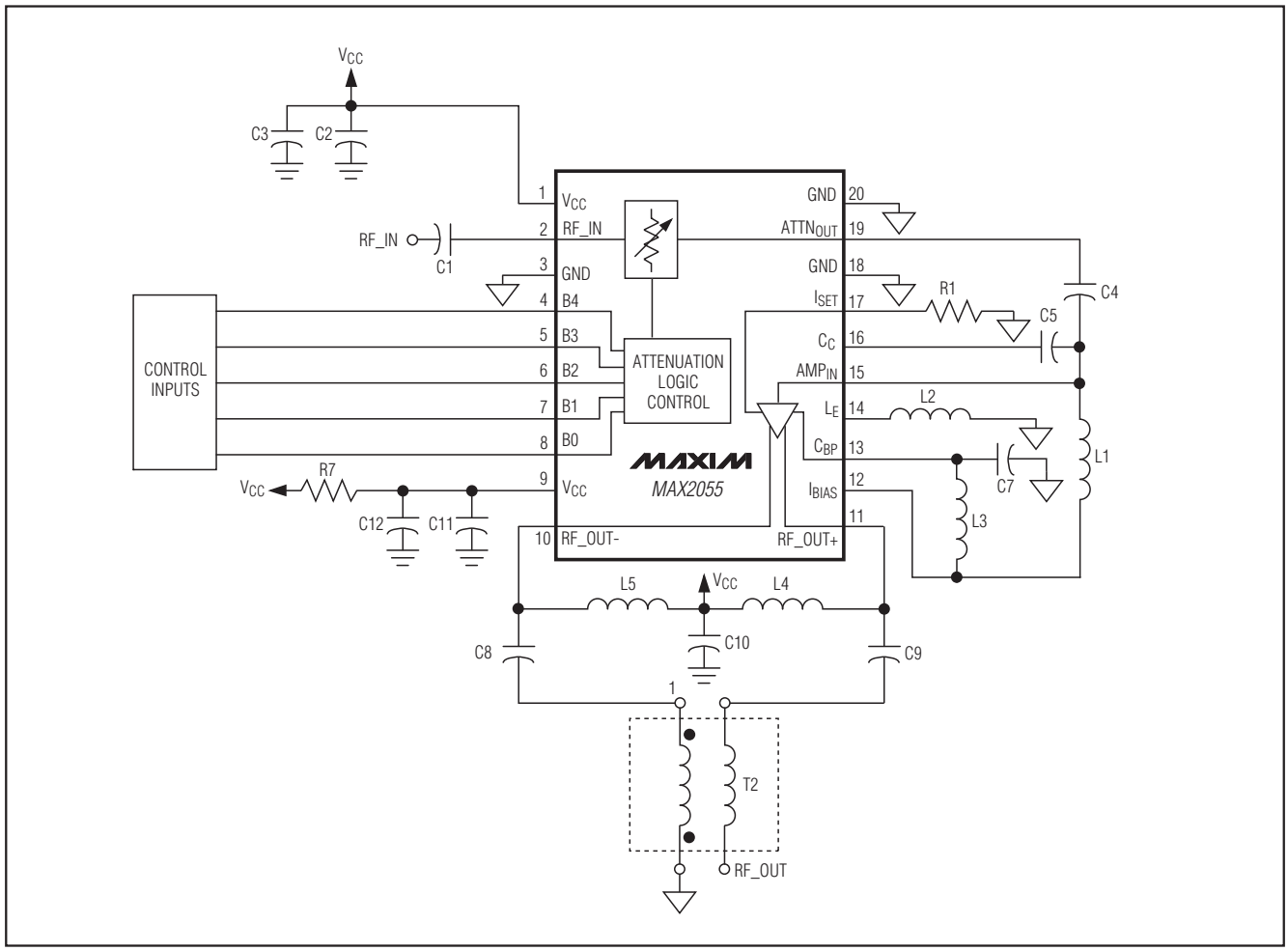


图2. 低成本应用电路

单端至差分放大器

MAX2055集成了一个单端至差分放大器，该放大器采用负反馈拓扑结构，标称增益为22dB。放大器经过优化用于30MHz至300MHz的工作频率范围，具有高输出3阶交调点(OIP3)。通过选择偏置电流可优化放大器的IP3，当R1为1.13kΩ (如果使用图2电路，则为909Ω)时，电流损耗为240mA，70MHz下的典型输出IP3为40dBm。共模电感L2可提供较高的共模抑制，并具有极好的幅度和相位平衡输出。L2用于处理电源电流，要求其直流电阻小于0.2Ω。

扼流电感

单端放大器输入和差分输出端口需要外部扼流电感。在输入端，在AMP_{IN} (第15引脚)和I_{BIAS} (第12引脚)之间连接一个330nH的偏置电感。在RF_OUT+ (第11引脚)及RF_OUT- (第10引脚)与V_{CC}之间连接680nH扼流电感，这些连接为放大器提供偏置电流。

布局考虑

合理的PCB设计对于RF/微波电路至关重要。RF信号线要尽可能短以降低损耗、辐射和寄生电感。为获得最佳性能，将接地引脚直接连接至封装下面的裸焊盘。该焊盘

数字控制、可变增益的差分ADC驱动器/放大器

需通过器件下面的多个过孔连接至电路板的地层，从而提供最佳的RF传导和散热路径。将器件封装底部的裸焊盘焊接至PCB的地平面。

PCB布局可参考MAX2055评估板，Gerber文件可从www.maxim-ic.com.cn网站申请。

电源旁路

合理的电源旁路对高频电路的稳定非常重要。采用1000pF和100pF电容旁路每个V_{CC}引脚，100pF电容要尽可能靠近器件放置。电阻R7有助于减小开关瞬态效应，如果对开关瞬态效应要求不严格，则无需R7。因此，第9引脚可直接连接至V_{CC}。

裸焊盘、RF散热考虑

采用20引脚TSSOP-EP封装的MAX2055，其EP提供了一条至管芯的低热阻路径。对于安装了该IC的PCB，通过该通道散热非常重要。此外，EP为该器件提供了一个低感抗的RF地回路。

建议将EP直接或通过一排电镀过孔焊接至PCB的地层。

将该焊盘焊接至地层对于有效散热也非常关键，尽可能铺设大面积的地平面。

芯片信息

TRANSISTOR COUNT: 325

PROCESS: BiCMOS

表3. 衰减设置与增益控制位的关系

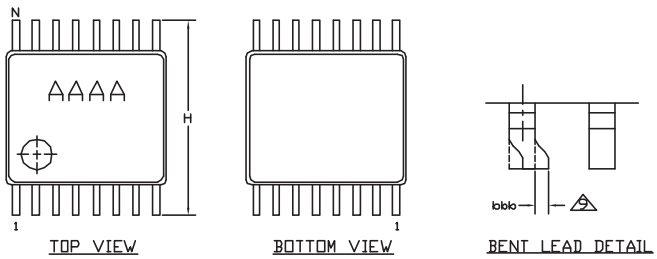
ATTENUATION	B4	B3*	B2	B1	B0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	X	0	0	0
17	1	X	0	0	1
18	1	X	0	1	0
19	1	X	0	1	1
20	1	X	1	0	0
21	1	X	1	0	1
22	1	X	1	1	0
23	1	X	1	1	1

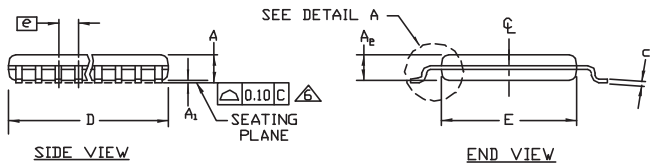
**使能B4会禁止B3，最小衰减为16dB。*

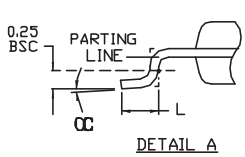
封装信息

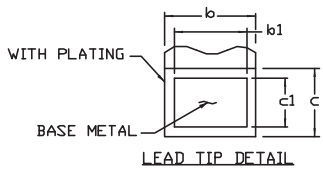
(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外形信息，请查询 **www.maxim-ic.com.cn/packages**。)

TSSOP4.40mm.EPS









SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1, U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1, U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2, U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1, U28-2, U28-3	9.60	9.80	.378	.386

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	I	1/1

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