TQL9044

1500 – 2700 MHz Bypass LNA

Applications

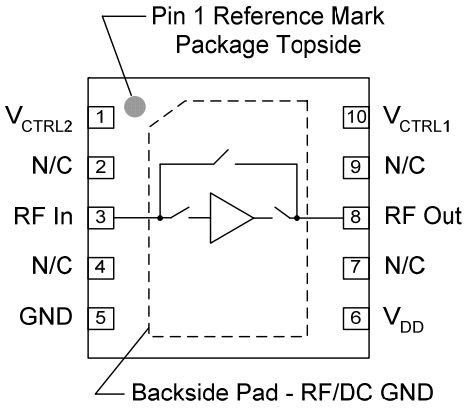
- Base Station Receivers
- Tower Mount Amplifiers
- Repeaters
- FDD-LTE, TDD-LTE, WCDMA
- General Purpose Wireless

10-pin 3 x 3 mm DFN Package

Product Features

- 1.5 – 4.0 GHz Operational bandwidth
- LNA with integrated bypass mode
- Ability to turn LNA and bypass mode OFF
- Ultra low noise, 0.6 dB at 1.9 GHz
- 19.4 dB Gain at 1.9 GHz
- +34.5 dBm Output IP3 in LNA Mode
- +36 dBm Input IP3 in Bypass Mode
- Internally matched
- Positive supply only, +3.3 to +5 V
- 3x3 mm 10-pin DFN plastic package

Functional Block Diagram



General Description

The TQL9044 is a high-linearity, ultra-low noise gain block amplifier with a bypass mode functionality integrated in the product. At 1.9 GHz, the amplifier typically provides 19.4 dB gain, +34.5 dBm OIP3, and 0.6 dB noise figure while drawing 70 mA current from a +5 V supply. The component also provides high linearity in the bypass mode with +36 dBm IIP3.

The TQL9044 is internally matched using a high performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias to maintain high performance over temperature.

The TQL9044 covers the 1.5 – 2.7 GHz frequency band and is targeted for wireless infrastructure. The TQL9044 is packaged in a 3 x 3 mm and is pin compatible with the 0.5 – 2.0 GHz TQL9042 and 1.5 – 2.7GHz TQL9043.

Pin Configuration

Pin No.	Label
1	V_{CTRL2}
2, 4, 7, 9	N/C
3	RFin
5	GND
6	V_{DD}
8	RFout
10	V_{CTRL1}
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
TQL9044	1500−4000 MHz Bypass LNA
TQL9044-PCB	1500−2700 MHz Evaluation Board

Standard T/R size = 2500 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150 °C
Drain Voltage (V_{DD})	+7 V
Input Power (CW)	+22 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_{DD})	+3.3	+5.0	+5.25	V
Operating Temp. Range	−40		+85	°C
T_{ch} (for>10^6 hrs MTTF)			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp.=+25°C.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1500		2700	MHz
Test Frequency			2600		MHz
Gain	LNA ON, Bypass OFF		17.0		dB
Input Return Loss	LNA ON, Bypass OFF		6.6		dB
Output Return Loss	LNA ON, Bypass OFF		10		dB
Noise Figure	LNA ON, Bypass OFF		0.8		dB
Output P1dB	LNA ON, Bypass OFF		+20		dBm
Output IP3	LNA ON, Bypass OFF, Pout=+5 dBm/tone, Δf=1 MHz		+34.3		dBm
Insertion Loss	LNA OFF, Bypass ON		1.3		dB
Return Loss	LNA OFF, Bypass ON		15		dB
Input IP3	LNA OFF, Bypass ON Pin=+6 dBm/tone, Δf=1 MHz		+35.6		dBm
Isolation	LNA OFF, Bypass OFF		13		dB
Control Voltage, V_1, V_2 (1)	V_{IH}	2.4		V_{DD}	V
	V_{IL}	0		0.4	V
Current, I_D	Bypass OFF		70		mA
	Bypass ON		3		mA
Switching Speed	Bypass to LNA Mode		1.48		µs
	LNA to Bypass Mode		70		ns
Thermal Resistance, θ_{jc}	Channel to case		TBD		°C/W

Notes:
1. These voltages are reference at the turrets labelled V1 and V2 on the circuit schematic on page 3.

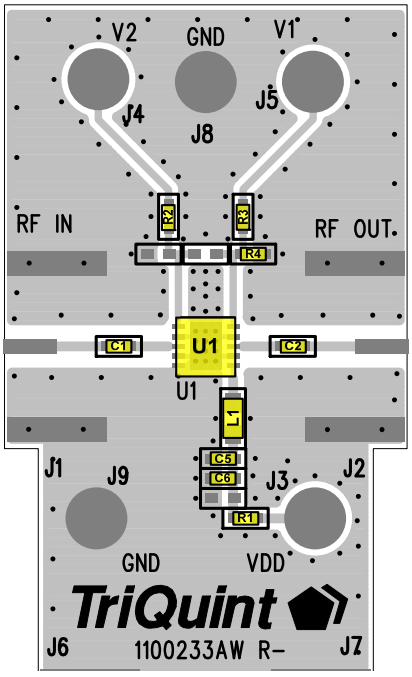
Control Truth Table

V_{CTRL2}	V_{CTRL1}	State
Low	High	LNA OFF, Bypass OFF
High	High	LNA OFF, Bypass ON
Low	Low	LNA ON, Bypass OFF
High	Low	Reserved (Do not use)

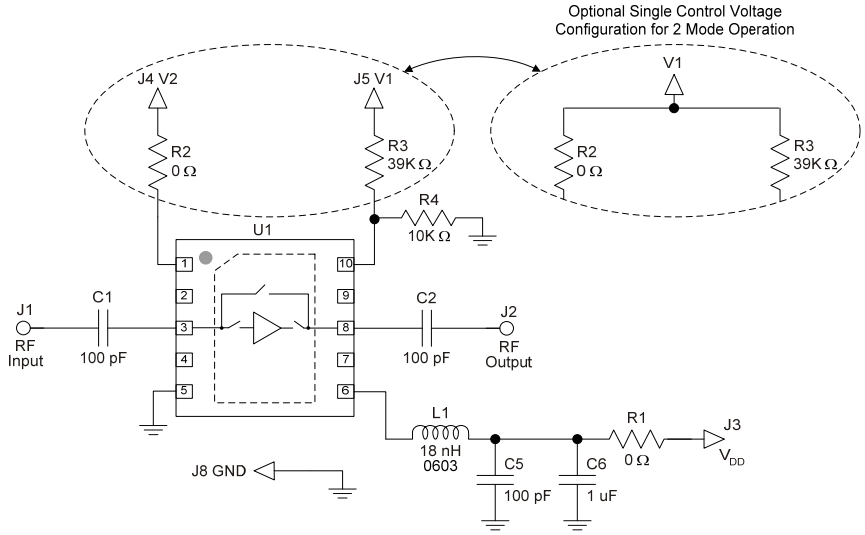
Control Voltage Limits (at device pins)

	State	Bias Condition
Vctrl1	Low	≤ 0.1 V
	High	≥ 0.52 V
Vctrl2	Low	≤ 0.4 V
	High	≥ 1.3 V

TQL9044-PCB Evaluation Board



See Evaluation Board PCB Information section for PCB material and stack-up.



Note:

If a TQL9044 application requires only two operational modes, LNA and bypass, the modes may be set using a single control voltage with the control lines tied together as shown above right. The corresponding truth table is shown below.

Control Truth Table – 2 Mode Operation

V_1	State
1	LNA OFF, Bypass ON
0	LNA ON, Bypass OFF

Bill of Material – TQL9044-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	Bypass LNA	TriQuint	TQL9044
C1, C2, C3, C4, C5	100 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H101J
C6	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	
R1, R2	0 Ω	RES, 0402, +/-5%, 1/10W	various	
R3	39K	RES, 0402, +/-5%, 1/10W	various	
R4	10K	RES, 0402, +/-5%, 1/10W	various	
L1	18 nH	IND, 0603, +/-5%	Coilcraft	0603CS-18NXJL

Power-up and Power-down Sequencing

		V_{DD}	V_{CTRL1} & V_{CTRL2}
LNA ON, Bypass OFF	Power-up	1st	2nd
	Power-down	1st	2nd
LNA OFF, Bypass ON	Power-up	1st	2nd
	Power-down	1st	2nd

Typical Performance (LNA Mode)

Test conditions unless otherwise noted: V_{DD} = +5 V, I_D = 70 mA, Temp.=+25 °C.

Parameter	Typical Value						Units
Frequency	1700	1900	2300	2500	2600	2700	MHz
Gain	20.2	19.4	18	17.3	17	16.7	dB
Noise Figure	0.55	0.6	0.63	0.7	0.8	0.8	dB
Input Return Loss	6.0	6.2	6.4	6.4	6.6	6.6	dB
Output Return Loss	9.8	9.8	9.9	10	10.1	10.2	dB
Output P1dB	+19.8	+20.4	+20	+20	+19.9	+19.8	dBm
OIP3 (Pout/tone=+5 dBm, Δf = 1 MHz)	+34.6	+34.5	+34.5	+34.5	+34.3	+34.8	dBm

Typical Performance (Bypass Mode)

Test conditions unless otherwise noted: V_{DD} = +5 V, I_d = 3 mA, Temp.=+25 °C.

Parameter	Typical Value						Units
Frequency	1700	1900	2300	2500	2600	2700	MHz
Insertion Loss	1	1	1.1	1.2	1.3	1.4	dB
Input Return Loss	16.3	16	15.6	15.5	15.4	15.1	dB
Output Return Loss	19.2	19.8	19.6	19.7	19.4	19	dB
Input IP3 (Pin/tone=+6 dBm, Δf = 1 MHz)	+36.1	+36.2	+36.4	+35.1	+35.6	+35.5	dBm

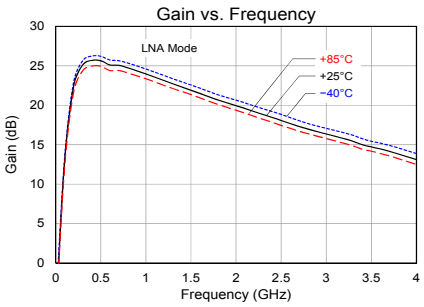
Typical Performance (LNA OFF, Bypass OFF Mode)

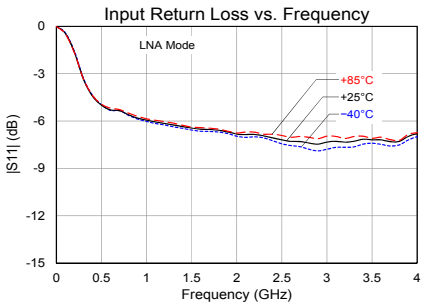
Test conditions unless otherwise noted: V_{DD} = +5 V, Temp.=+25 °C.

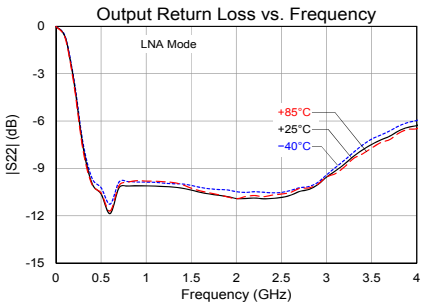
Parameter	Typical Value						Units
Frequency	1700	1900	2300	2500	2600	2700	MHz
Isolation	8.7	9.5	11.2	12.2	13	13.5	dB

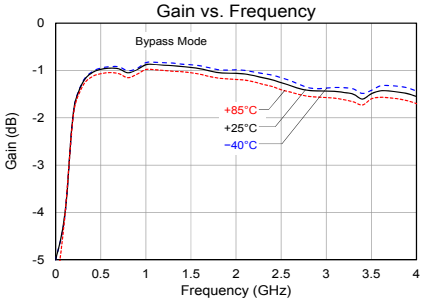
Performance Plots

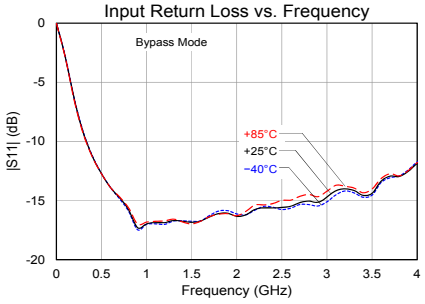
Test conditions unless otherwise noted: V_{DD} = +5 V, I_D =70 mA

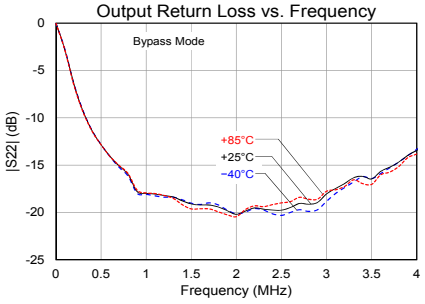


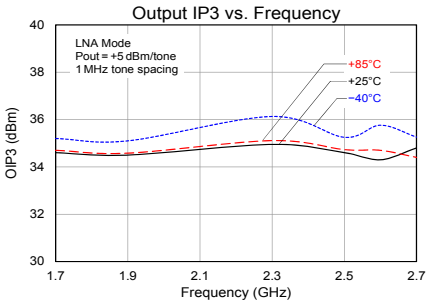


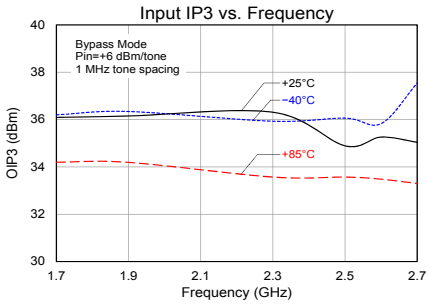


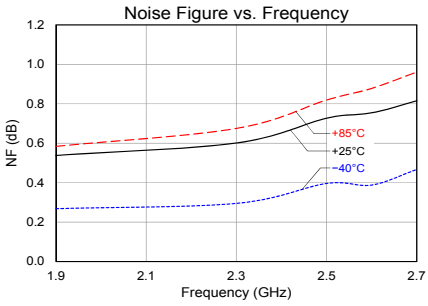


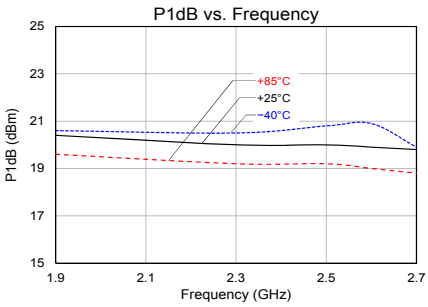


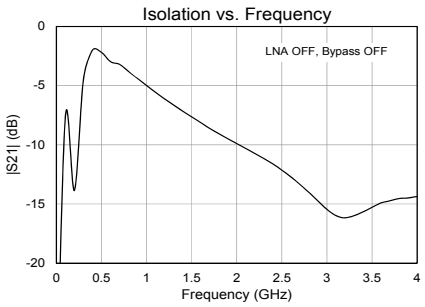


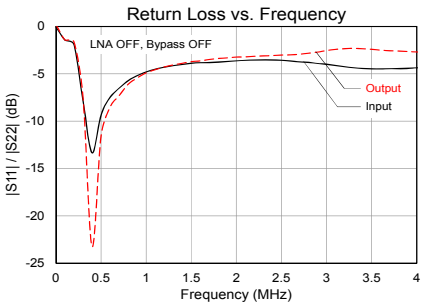




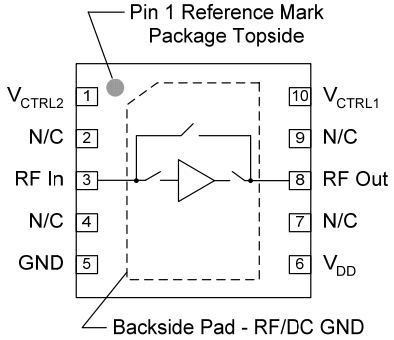








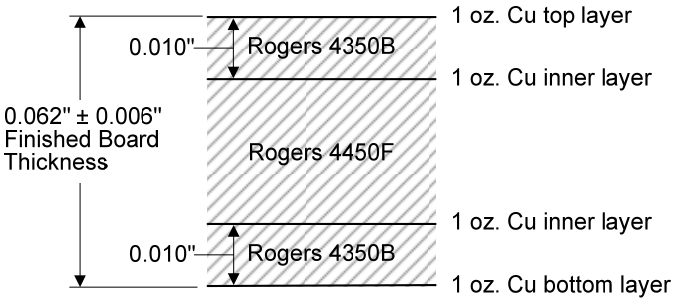
Pin Configuration and Description



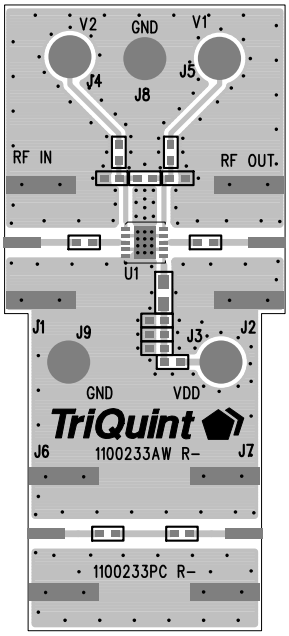
Pin No.	Label	Description
1	V_{CTRL2}	Control pin for bypass mode and LNA mode. Internal resistor divider. Refer to truth table.
2, 4, 7, 9	N/C	No internal connection. Provide grounded PCB land pads for mounting integrity.
3	RFin	RF input pin. DC block required.
5	GND	RF/DC Ground pin.
6	V_{DD}	Supply voltage pin.
8	RFout	RF output pin. DC block required.
10	V_{CTRL1}	Control pin for bypass mode and LNA mode. Requires external resistor divider. Refer to truth table.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

Evaluation Board PCB Information

TriQuint PCB 1100233 Material and Stack-up



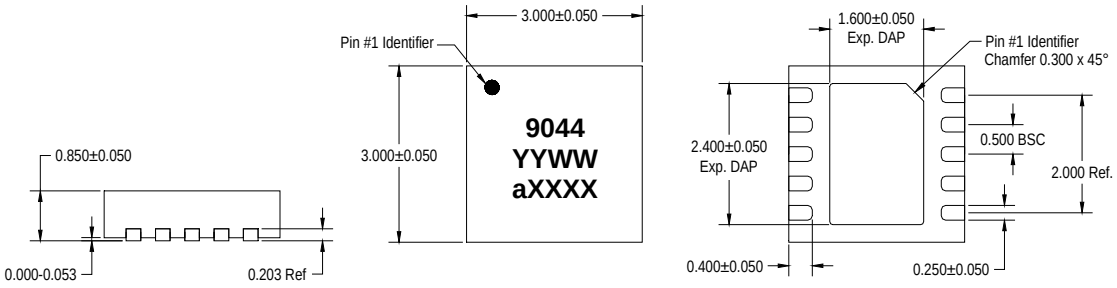
50 ohm line dimensions: width = .020”, spacing = .032”



Mechanical Information

Package Marking and Dimensions

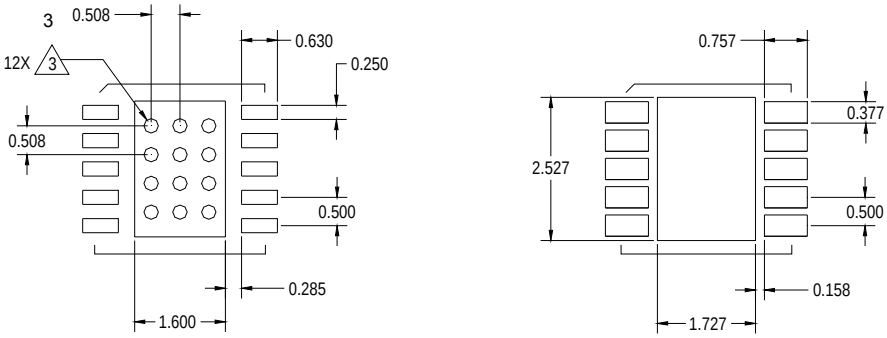
Marking: Part number – 9044
Year/Week – YYWW
Lot Code – aXXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-229.
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity

Caution! ESD-Sensitive Device

ESD Rating: Class 1A
Voltage: ≥250V to 500V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: ≥ 1000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating: Level 1
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes.

Package contact plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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