High Power 44 W Peak, Silicon SPDT, Reflective Switch, 0.7 GHz to 3.5 GHz

Preliminary Technical Data

ADRF5130

FEATURES

- Reflective, 50 Ω design
- Low insertion loss: 0.6 dB typical at 2 GHz
- High isolation: 50 dB typical at 2 GHz
- High power handling
  - Continuous average power: 43 dBm
  - Peak power: 46.5 dBm
- High linearity
  - 0.1 dB compression (P0.1dB): >46 dBm typical
  - Input third-order intercept (IP3): 68 dBm typical at 2 GHz
- ESD ratings
  - Human body model (HBM): 2 kV, Class 2
  - Charged device model (CDM): TBD
- Single positive supply
  - V_{DD}: 5 V
- Positive control, TTL compatible
  - V_{CTL}: 0 V or 5 V
- 24-lead, 4 mm × 4 mm LFCSP package (16 mm²)

APPLICATIONS

- Cellular/4G infrastructure
- Wireless infrastructure
- Military and high reliability applications
- Test equipment
- Pin diode replacement

FUNCTIONAL BLOCK DIAGRAM

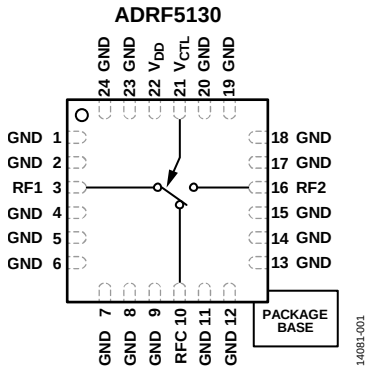

Figure 1.

GENERAL DESCRIPTION

The ADRF5130 is a high power, reflective, 0.7 GHz to 3.5 GHz, silicon, single-pole, double-throw (SPDT) switch in a leadless, surface-mount package. The switch is ideal for high power and cellular infrastructure applications, like long-term evolution (LTE) base stations. The ADRF5130 has high power handling of 43 dBm (typical), a low insertion loss of 0.6 dB, input linearity of 68 dBm (typical) third-order intercept, and 0.1 dB compression point (P0.1dB) of 46 dBm. On-chip circuitry operates at a single, positive supply voltage of 5 V and typical bias current of 1 mA, making the ADRF5130 an ideal alternative to pin diode-based switches.

The device comes in a RoHS compliant, compact, 24-lead, 4 mm × 4 mm LFCSP package.

Rev. PrA

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SPECIFICATIONS

V_{DD} = 5 V, V_{CTL} = 0 V or V_{DD}, T_A = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		0.7		3.5	GHz
INSERTION LOSS	0.7 GHz to 2.0 GHz		0.6		dB
	2.0 GHz to 3.5 GHz		0.7		dB
ISOLATION					
RFC to RF1/RF2 (Worst Case)	0.7 GHz to 2.0 GHz		50		dB
	2.0 GHz to 3.5 GHz		46		dB
RF1 to RF2 (Worst Case)	0.7 GHz to 2.0 GHz		51		dB
	2.0 GHz to 3.5 GHz		41		dB
RETURN LOSS					
RFC	0.7 GHz to 2.0 GHz		23		dB
	2.0 GHz to 3.5GHz		17		dB
RFC to RF1/RF2	0.7 GHz to 2.0 GHz		21		dB
	2.0 GHz to 3.5 GHz		17		dB
SWITCHING SPEED					
Rise and Fall Time (t_{RISE}, t_{FALL})	90% to 10% of RF output		155		ns
On and Off time (t_{ON}, t_{OFF})	50% V_{CTL} to 10% to 90% of RF output		750		ns
Radio Frequency (RF) SETTLING TIME	50% V_{CTL} to 0.1 dB margin of final RF output		TBD		ns
INPUT POWER					
1 dB Compression (P1dB)			TBD		dB
0.1 dB Compression (P0.1dB)			46		dB
INPUT THIRD-ORDER INTERCEPT (IP3)	Two-tone input power = 25 dBm/tone				
	0.7 GHz to 2 GHz		68		dBm
	2 GHz to 3.5 GHz		65		dBm
RECOMMENDED OPERATING CONDITIONS	0.7 GHz to 3.5 GHz				
Bias Voltage Range (V_{DD})		4.5		5.4	V
Control Voltage Range (V_{CTL})		0		V_{DD}	V
Maximum RF Input Power					
T_{CASE} = 105°C	Continuous wave (CW)			41	dBm
	8 dB peak to average ratio (PAR) LTE, average			TBD	dBm
	8 dB PAR LTE, single event (<10 sec), average			TBD	dBm
T_{CASE} = 85°C	CW			43	dBm
	8 dB PAR LTE, average			38.5	dBm
	8 dB PAR LTE, single event (<10 sec), average			44	dBm
T_{CASE} = 25°C	CW			TBD	dBm
	8 dB PAR LTE, average			TBD	dBm
	8 dB PAR LTE, single event (<10 sec), average			TBD	dBm
T_{CASE} = −40°C	CW			TBD	dBm
	8 dB PAR LTE, average			TBD	dBm
	8 dB PAR LTE, single event (<10 sec), average			TBD	dBm
Case Temperature Range (T_{CASE})		−40		+105	°C
DIGITAL INPUT CONTROL VOLTAGE	V_{DD} = 4.5 V to 5.4 V, T_{CASE} = −40°C to +105°C, at <1 µA typical				
Low (V_{IL})		0		0.8	V
High (V_{IH})		1.3		5.0	V
SUPPLY CURRENT (I_{DD})	V_{DD} = 5 V		1.06		mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Bias Voltage Range (V_{DD})	−0.3 V to +5.5 V
Control Voltage Range (V_{CTL})	−0.3 V to +5.5 V
RF Input Power[1]	46.5 dBm
Channel Temperature	135°C
Storage Temperature Range	−65°C to +150°C
Peak Reflow Temperature	260°C
Thermal Resistance (Channel to Package Bottom)	17°C/W
ESD Sensitivity	
HBM	2 kV (Class 2)
CDM	TBD

[1] For recommended operating conditions, see Table 1.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

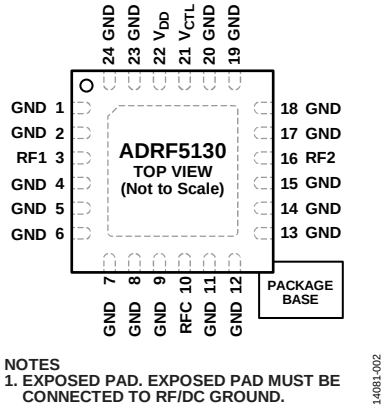

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 17, 18, 19, 20, 23, 24	GND	Ground. The package bottom has an exposed metal pad that must connect to the printed circuit board (PCB) RF ground. See Figure 3 for the GND interface schematic.
3	RF1	RF Port 1. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
10	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
16	RF2	RF Port 2. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required on this pin.
21	V_{CTL}	Control Input. See Figure 4 for the V_{CTL} interface schematic. Refer to Table 4 and the recommended digital input control voltage range in Table 1.
22	V_{DD}	Supply Voltage.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

Table 4. Truth Table

	Signal Path State	
Control Input, V_{CTL} State	**RFC to RF1**	**RFC to RF2**
Low	Off	On
High	On	Off

INTERFACE SCHEMATICS

Figure 3. Ground Interface

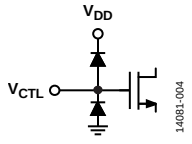

Figure 4. Control Interface

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, ISOLATION, AND RETURN LOSS

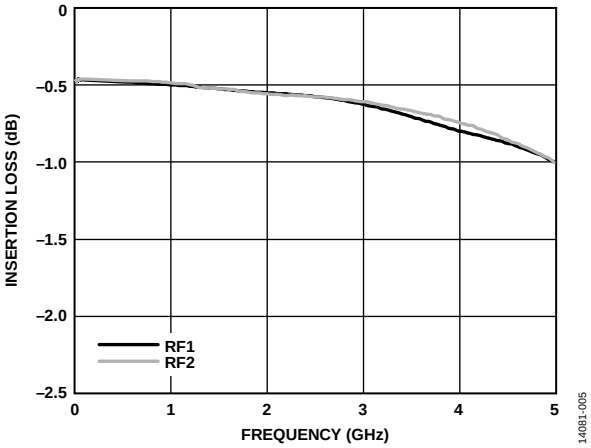

Figure 5. Insertion Loss of RF1 and RF2 vs. Frequency at V_{DD} = 5 V

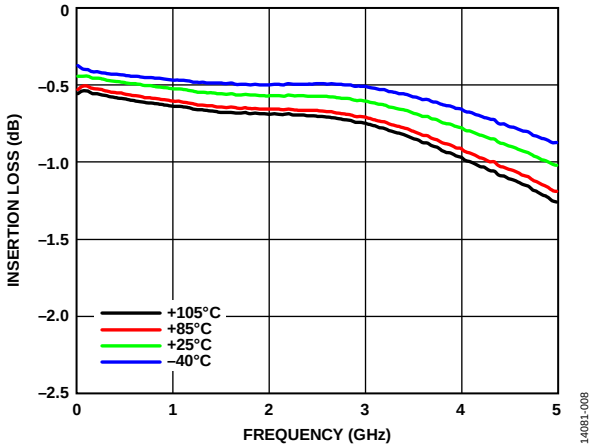

Figure 8. Insertion Loss vs. Frequency, Over Temperature at V_{DD} = 5 V

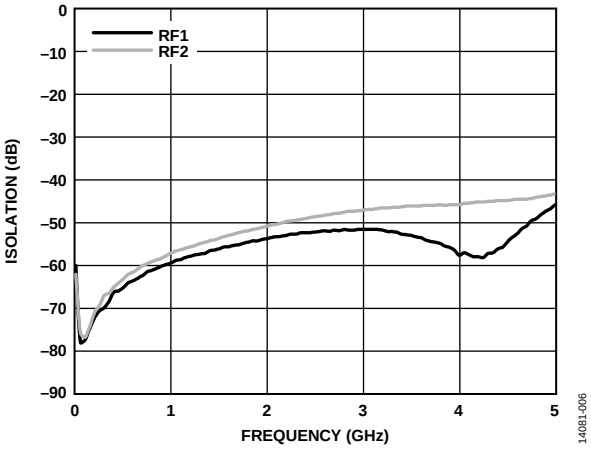

Figure 6. Isolation Between RFC and RF1/RF2 vs. Frequency at V_{DD} = 5 V

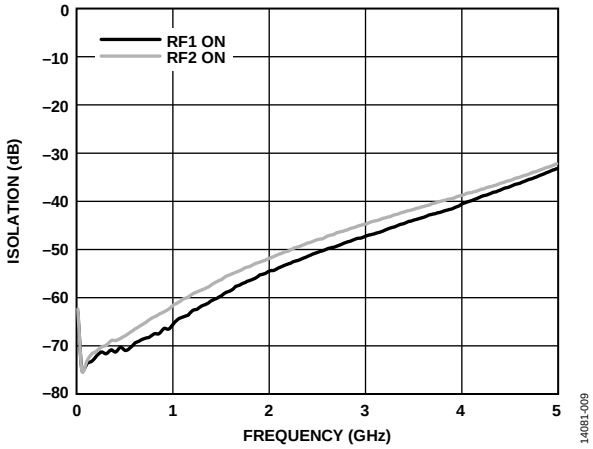

Figure 9. Isolation Between RF1 and RF2 vs. Frequency at V_{DD} = 5 V, Switch Mode On

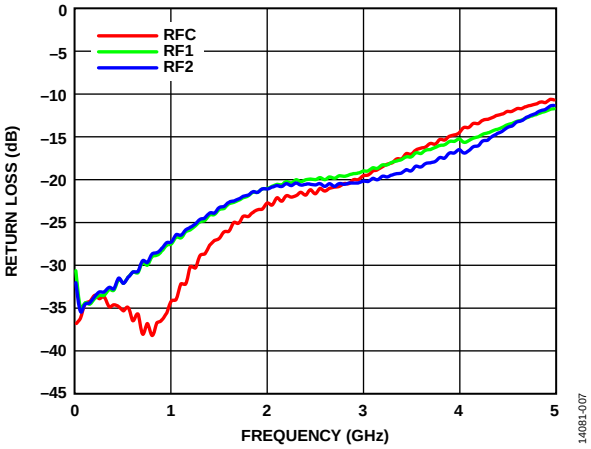

Figure 7. Return Loss vs. Frequency at V_{DD} = 5 V

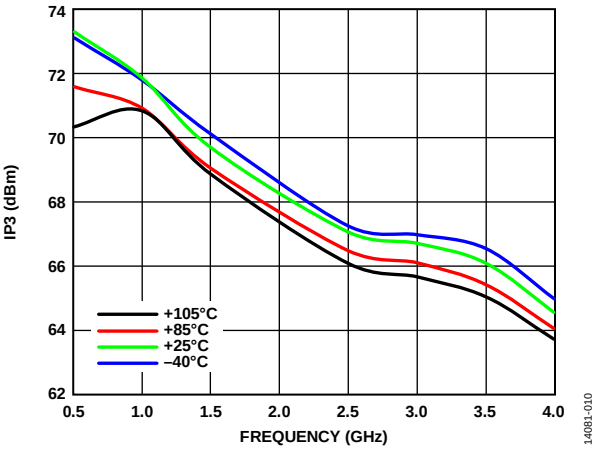

Figure 10. IP3 vs. Frequency over Temperature, V_{DD} = 5 V

THEORY OF OPERATION

The ADRF5130 requires a single-supply voltage applied to the V_{DD} pin. Bypass capacitors are recommended on the supply line to minimize RF coupling.

The ADRF5130 is controlled via a digital control voltage applied to the V_{CTL} pin. A small bypassing capacitor is recommended on these digital signal lines to improve the RF signal isolation.

The ADRF5130 is internally matched to 50 Ω at the RF input port (RFC) and the RF output ports (RF1 and RF2); therefore, no external matching components are required. The RFx pins are dc-coupled, and dc blocking capacitors are required on the RF lines. The design is bidirectional; the input and outputs are interchangeable.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up V_{DD}.
3. Power up the digital control input. Powering the digital control input before the V_{DD} supply can inadvertently forward bias and damage ESD protection structures.
4. Power up the RF input. Depending on the logic level applied to the V_{CTL} pin, one RF output port (for example, RF1) is set to on mode, by which an insertion loss path is provided from the input to the output, while the other RF output port (for example, RF2) is set to off mode, by which the output is isolated from the input.

Table 5. Switch Operation Mode

Digital Control Input, VCTL	Switch Mode	
	RFC to RF1	**RFC to RF2**
0	Off mode: the RF1 port is isolated from the RFC port and is internally terminated to a 50 Ω load to absorb the applied RF signals.	On mode: a low insertion loss path from the RFC port to the RF2 port.
1	On mode: a low insertion loss path from the RFC port to the RF1 port.	Off mode: the RF2 port is isolated from the RFC port and is internally terminated to a 50 Ω load to absorb the applied RF signals.

APPLICATIONS INFORMATION

Generate the evaluation printed circuit board (PCB) used in the application circuit shown in Figure 11 with proper RF circuit design techniques. Signal lines at the RF port must have a 50 Ω impedance, and the package ground leads and backside ground slug must connect directly to the ground plane, as shown in Figure 12. The evaluation board shown in Figure 12 is available from Analog Devices, Inc., upon request.

Table 6. Bill of Materials for ADRF5130-EVALZ Evaluation Board

Reference Designator	Description
J1 to J3	PCB mount SMA connector
C1 to C4, C7	100 pF capacitor, 0402 package
C6	1 µF capacitor, 0402 package
C5	1 nF capacitor, 0402 package
C8 to C15, C18 to C21	Do not insert
R1	0 Ω resistor, 0402 package
U1	ADRF5130 SPDT switch
PCB[1]	600-01532-00-2[2] evaluation PCB

[1] Circuit board material: Roger 4350 or Arlon 25FR.
[2] Reference this evaluation board number when ordering the complete evaluation board.

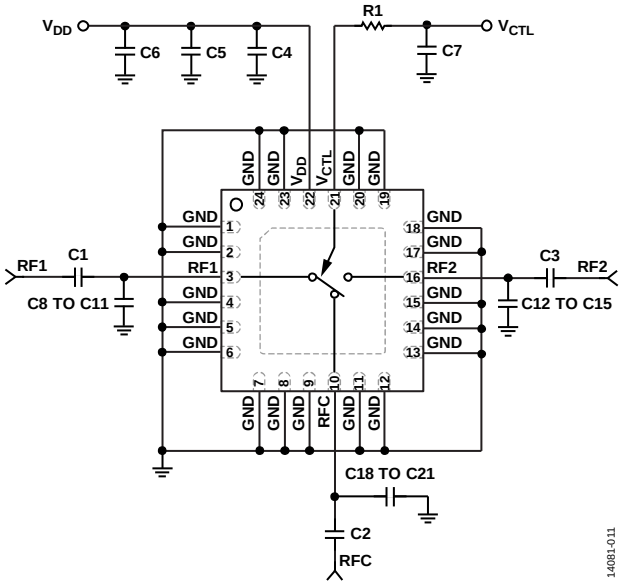

Figure 11. Application Circuit

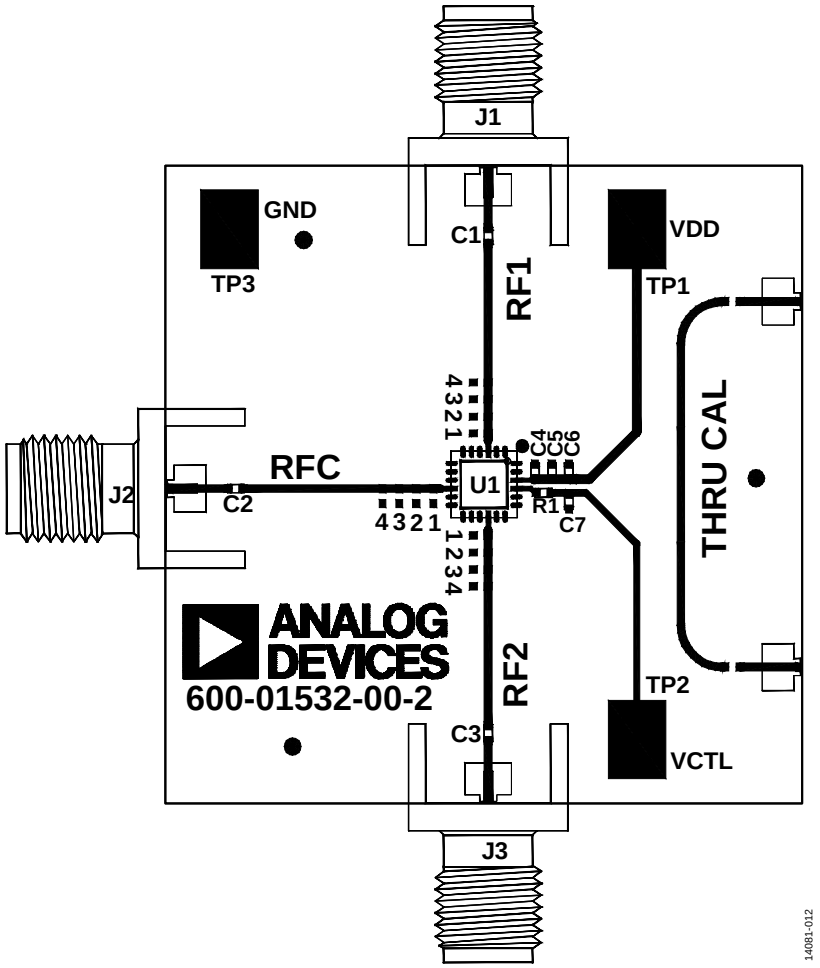

Figure 12. ADRF5130-EVALZ Evaluation Board

OUTLINE DIMENSIONS

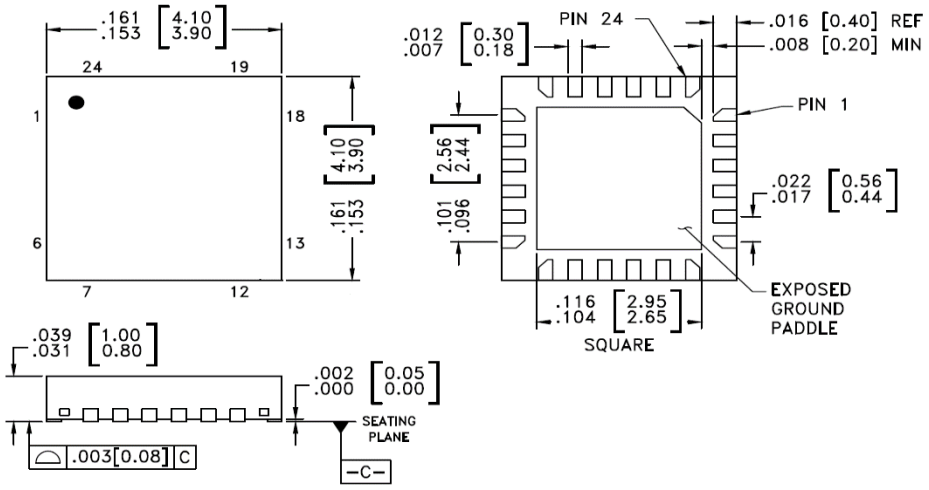

Figure 13. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.90 mm Package Height
MOD 4926
Dimensions shown in millimeters

PR14081-0-5/16(PrA)