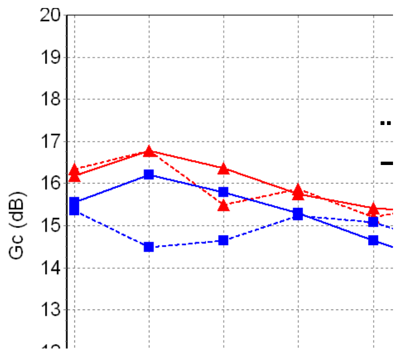
21-26.5GHz Integrated Down converter

GaAs Monolithic Microwave IC in SMD package

Description

The CHR3693-QDG is a multifunction chip, which integrates a balanced cold FET mixer, a time two multiplier, and a RF self biased LNA.
It is designed for a wide range of applications, typically commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate and air bridges.
It is supplied in lead-free SMD package.

Conversion gain (Inf. & Sup. Mode)



Main Features

- ■ Broadband performance 21-26.5GHz
- ■ 14dB gain
- ■ -5dBm input IP3
- ■ 18dBc image rejection
- ■ DC bias: Vd=4.0Volt@Id=160mA
- ■ 24LQFN4x4
- ■ MSL Level: 1

Main Electrical Characteristics

Tamb.= +25°C, Vdx=Vdl=4.0V, Vgx=-0.9V, Vgm=-0.7V

Symbol	Parameter	Min	Typ	Max	Unit
F_RF	RF frequency range	21		26.5	GHz
F_LO	LO frequency range	9		14	GHz
F_IF	IF frequency range	DC		3.5	GHz
Gc	Conversion gain	12	14		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

Electrical Characteristics

Tamb.= +25°C, Vdx=Vdl = +4.0V, Vgx=-0.9V, Vgm=-0.7V

Symbol	Parameter	Min	Typ	Max	Unit
F_RF	RF frequency range	21		26.5	GHz
F_LO	LO frequency range	9		14	GHz
F_IF	IF frequency range	DC		3.5	GHz
Gc	Conversion gain	12	14		dB
NF	Noise Figure for IF>0.1GHz		2	2.5	dB
P_LO	LO Input power		2	5	dBm
Img Sup	Image Suppression(1)	15	18		dBc
IIP3	Input IP3		-2		dBm
LO_RL	LO return loss		-9	-7	dB
RF_RL	RF return loss (21 to 24GHz) RF return loss (24 to 26.5GHz)		-12 -8	-7 -6	dB dB
LO/RF	Isolation LO → RF		45		dBc
2LO/RF	Isolation 2LO → RF		35		dBc
Id	Bias current(2) (Idl + Idx)	120	160	200	mA

(1) With external I/Q 90° hybrid coupler

(2) Typically, Idl= 90mA, Idx=70mA

These values are representative of onboard measurements as defined on the drawing at paragraph “Evaluation mother board”.

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Maximum drain bias voltage	4.5	V
Id	Maximum drain bias current	230	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
P_RF	Maximum RF input power (2)	10	dBm
P_LO	Maximum LO input power (2)	10	dBm
Tch	Maximum channel temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

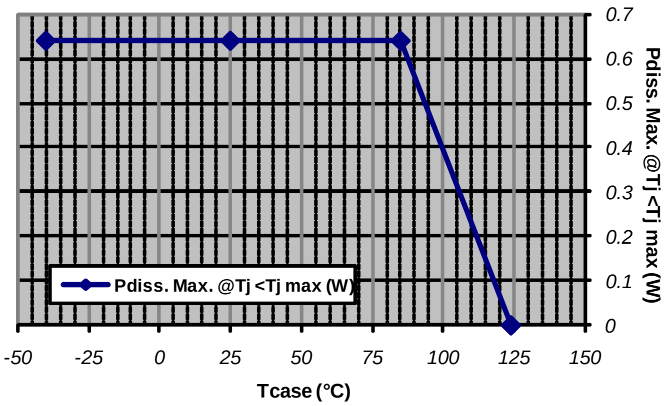
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

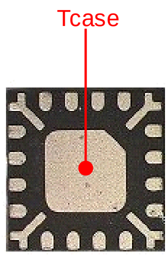
DEVICE THERMAL SPECIFICATION : Product name			
Recommended max. junction temperature (Tj max)	:	124	°C
Junction temperature absolute maximum rating	:	175	°C
Max. continuous dissipated power (Pdiss. Max.)	:	0.64	W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	16	mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<60	°C/W
Minimum Tcase operating temperature(3)	:	-40	°C
Maximum Tcase operating temperature(3)	:	85	°C
Minimum storage temperature	:	-55	°C
Maximum storage temperature	:	150	°C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the ***hottest junction*** *of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example : QFN 16L 3x3
Location of temperature
reference point (Tcase)
on package's bottom side

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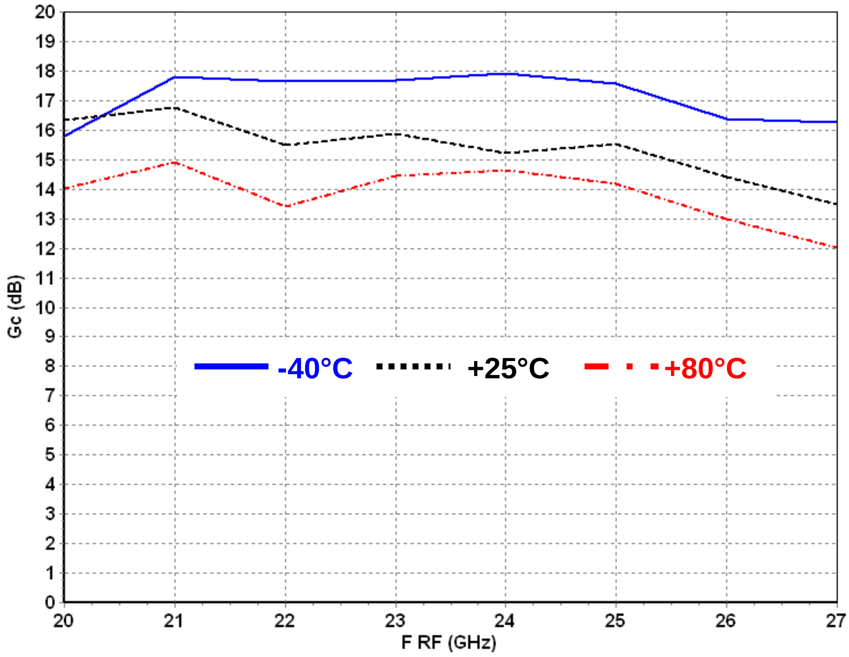
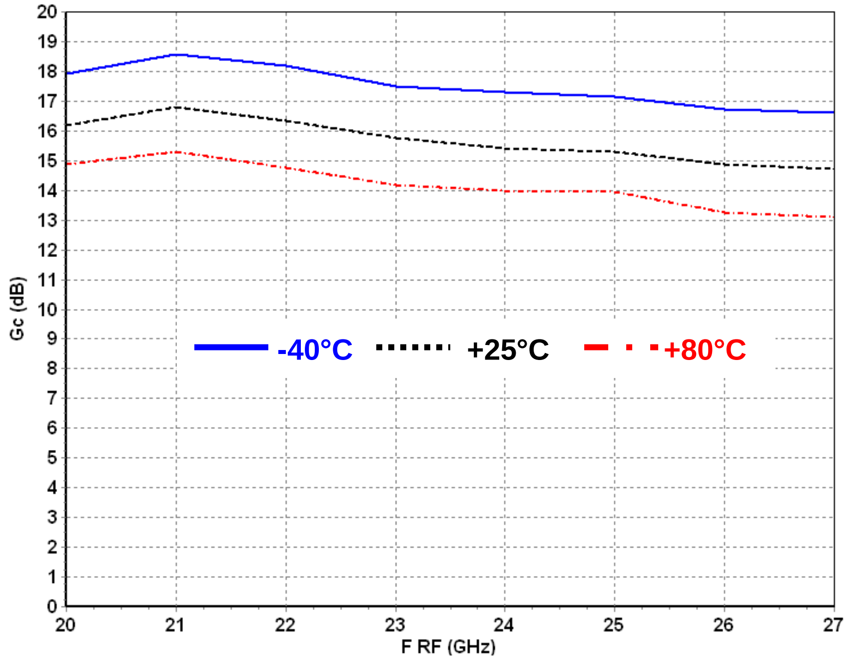
Typical Board Measurements

Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V
P_LO=2dBm, F_IF=2GHz
These values are representative of onboard measurements as defined on the drawing at page 12 (paragraph "Evaluation mother board") (in connector access planes).

Conversion Gain in infradyne mode versus frequency
F_RF = 2xF_LO-F_IF



Conversion Gain in supradyne mode versus frequency
F_RF = 2xF_LO+F_IF



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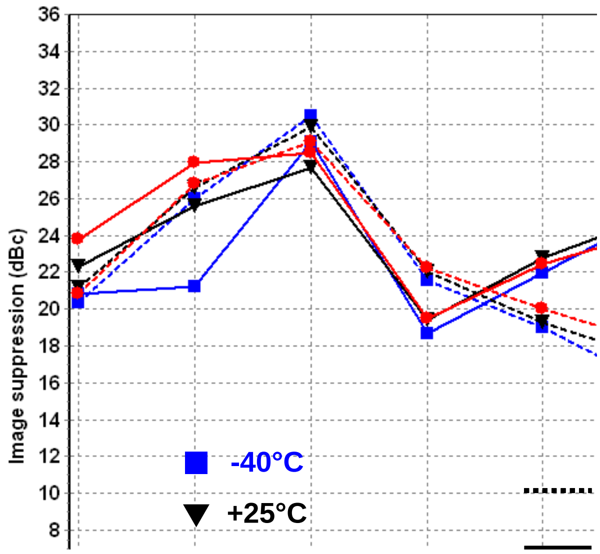
Typical Board Measurements

Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V
P_LO=2dBm, F_IF=2GHz

Image Frequency rejection (inf. & sup. Mode) @ -40, +25, +80°C



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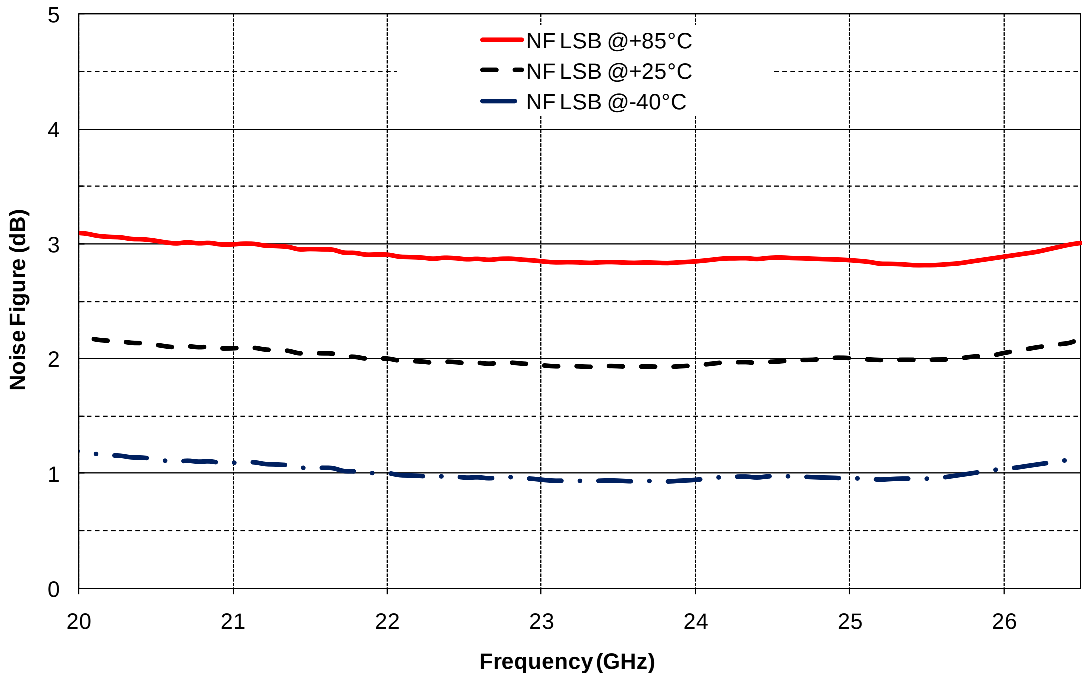
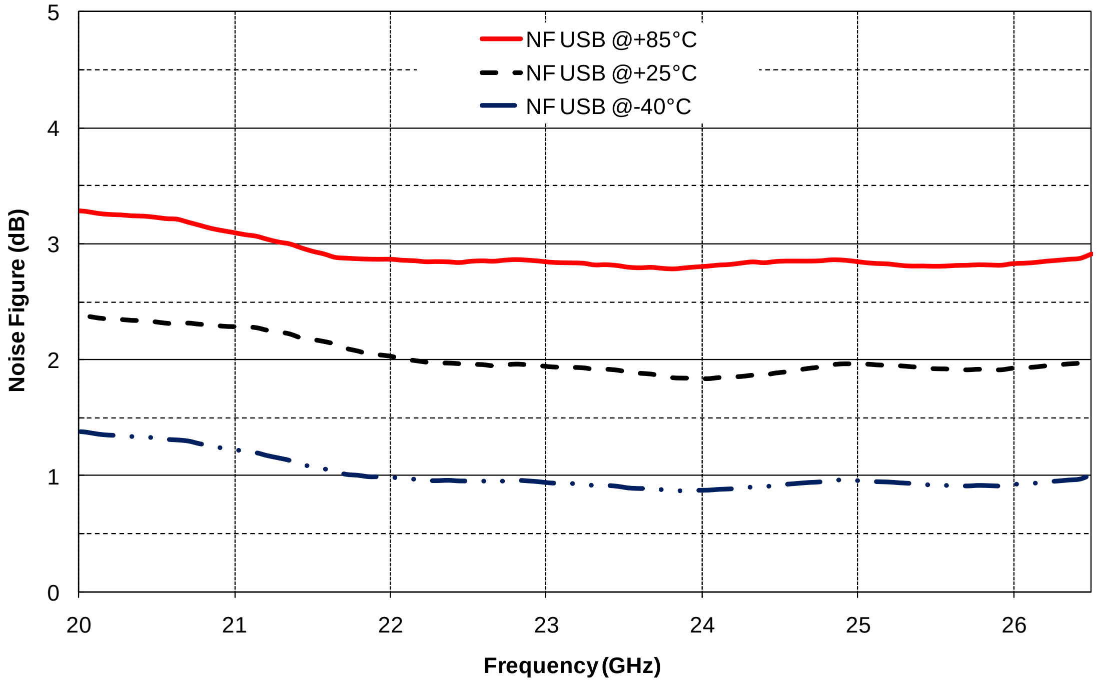
Typical Board Measurements

Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V
P_LO=2dBm, F_IF=2GHz
Board losses have been de-embedded (results in package access planes)

Noise Figure in infradyne mode versus frequency
F_RF = 2xF_LO-F_IF



Noise Figure in supradyne mode versus frequency
F_RF = 2xF_LO+F_IF



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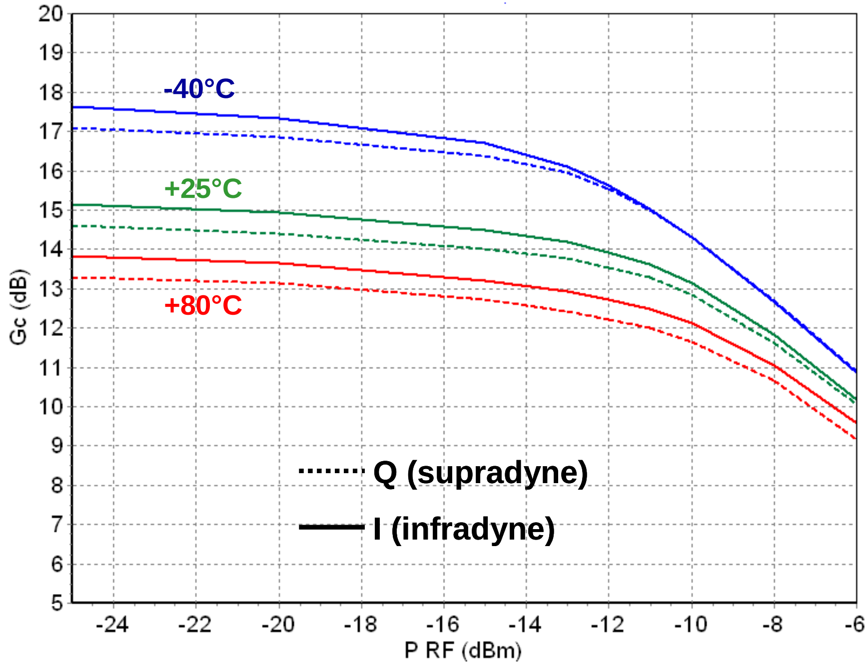
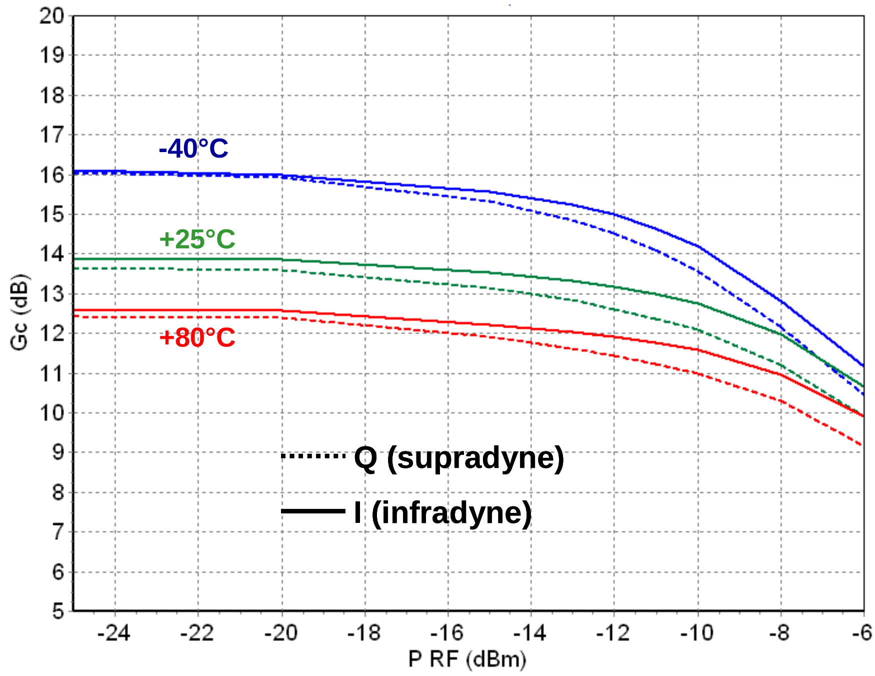
Typical Board Measurements

Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V
P_LO=2dBm

Compression versus PRF (infradyne and supradyne modes)
F_RF=21GHz & F_IF=3GHz



Compression versus PRF (infradyne and supradyne modes)
F_RF=26GHz & F_IF=2GHz



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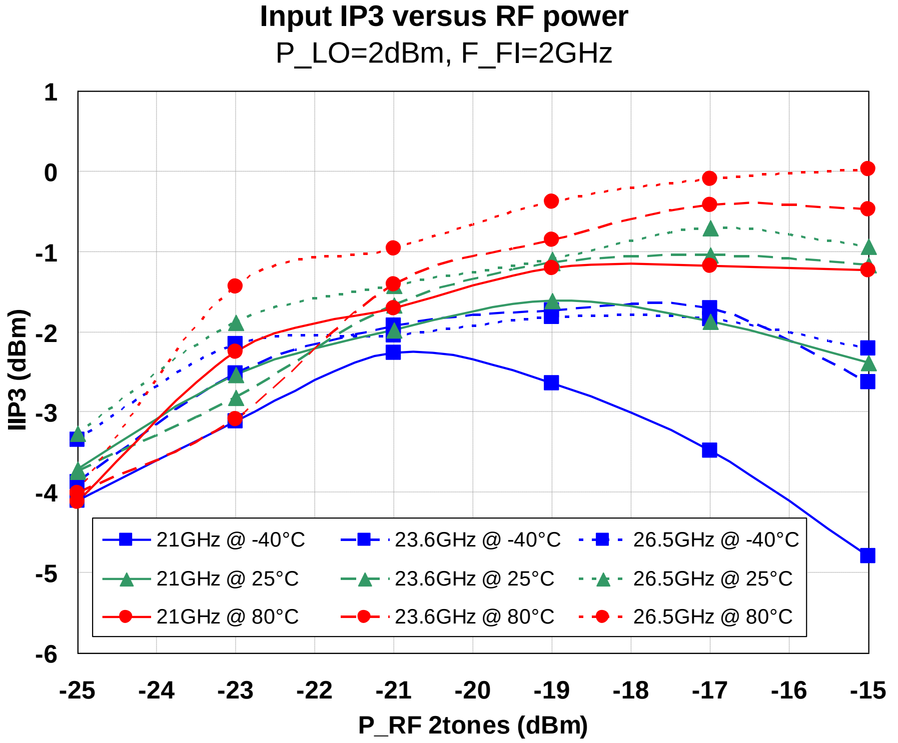
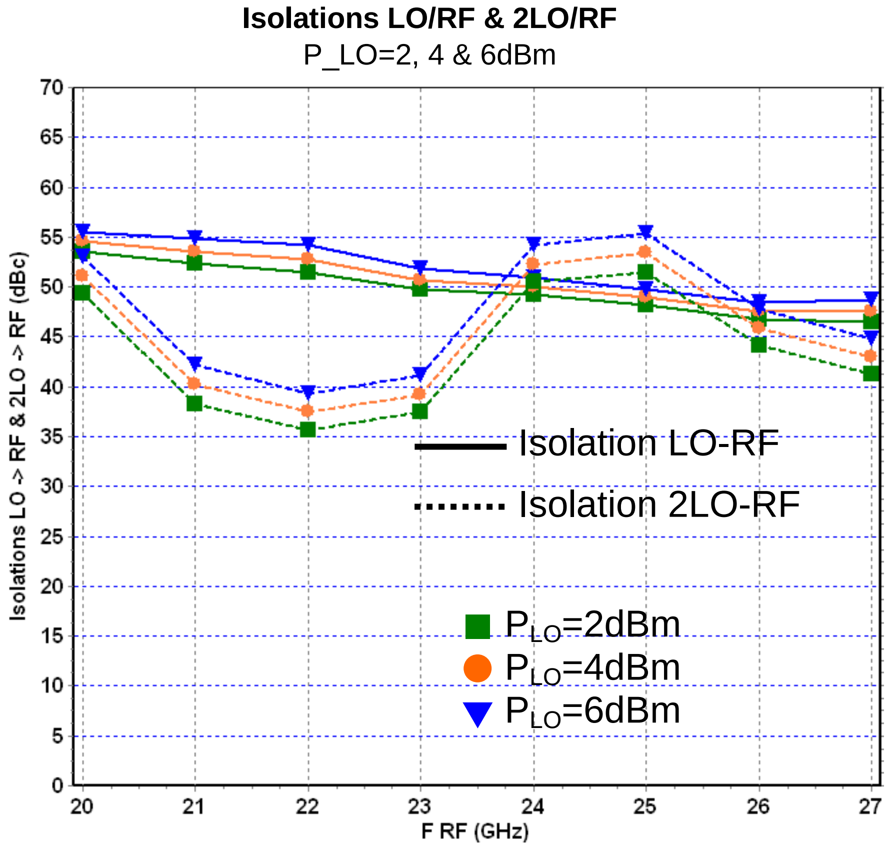
Typical Board Measurements

Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V





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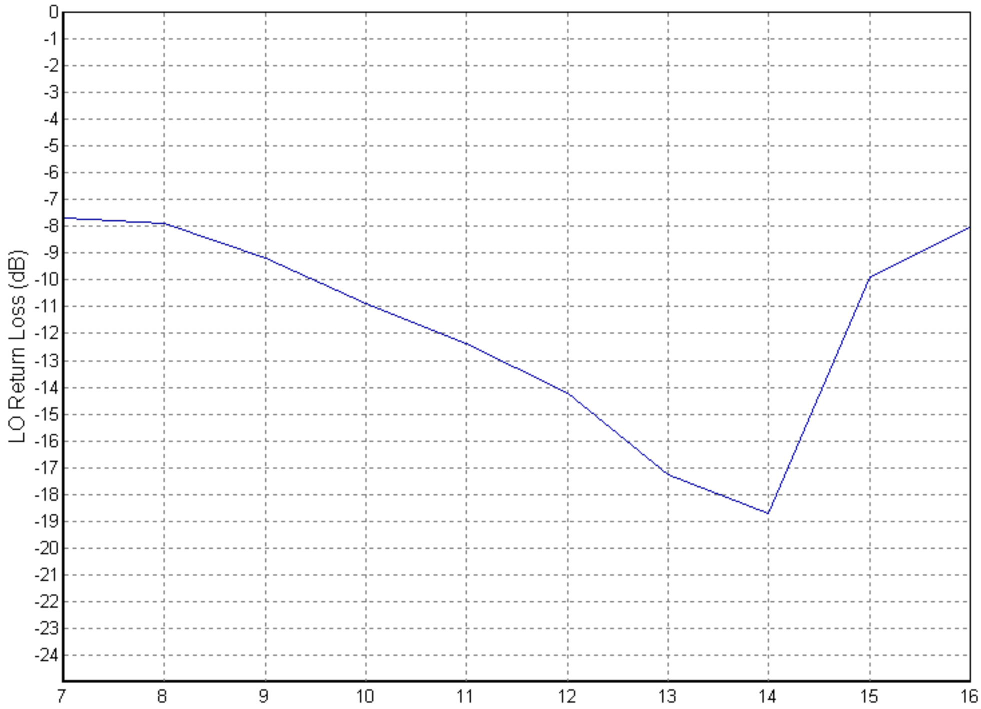
Typical Board Measurements

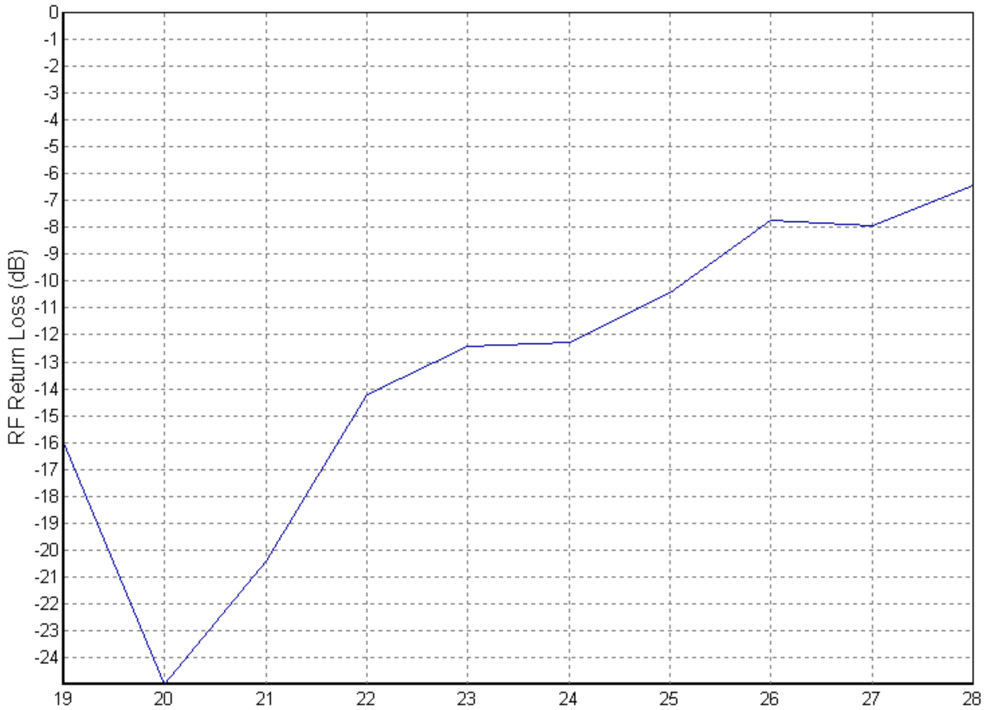
Tamb=25°C, Vdx=Vdl=4V, Typical Vgx=-0.9V & Vgm=-0.7V

LO Return Loss @ P_LO=0dBm



LO Freq (GHz)

RF Return Loss @ P_RF=-30dBm



RF Freq (GHz)

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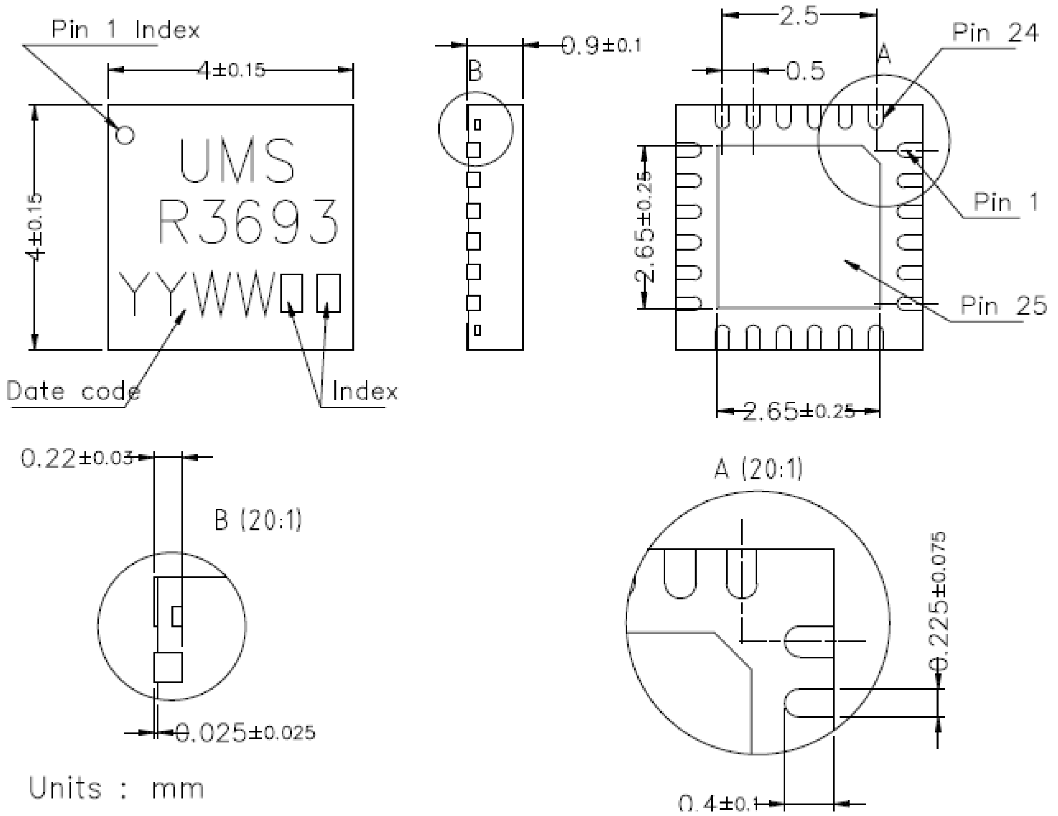
Package outline [1]



Matt tin, Lead Free	(Green)	1- NC	9- Vdx	17- Gnd[2]
Units :	mm	2- Gnd[2]	10- NC	18- NC
From the standard :	JEDEC MO-220	3- Gnd[2]	11- NC	19- I-IF out
	(VGGD)	4- RF in	12- Vgx	20- Gnd[2]
25-	GND	5- Gnd[2]	13- Gnd[2]	21- Gnd[2]
		6- Gnd[2]	14- Gnd[2]	22- Q-IF out
		7- Vdl	15- LO IN	23- NC
		8- Vgm	16- Gnd[2]	24- NC

[1] The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

[2] It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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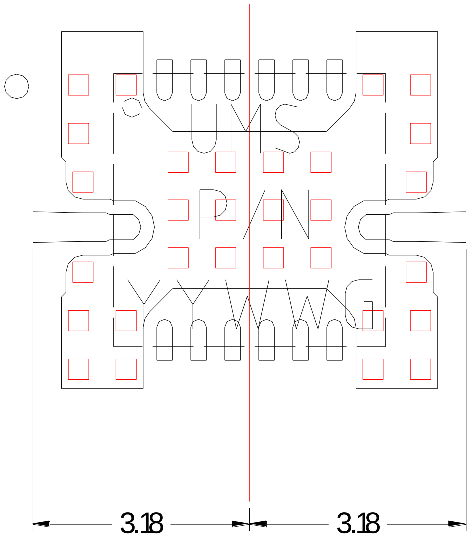
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



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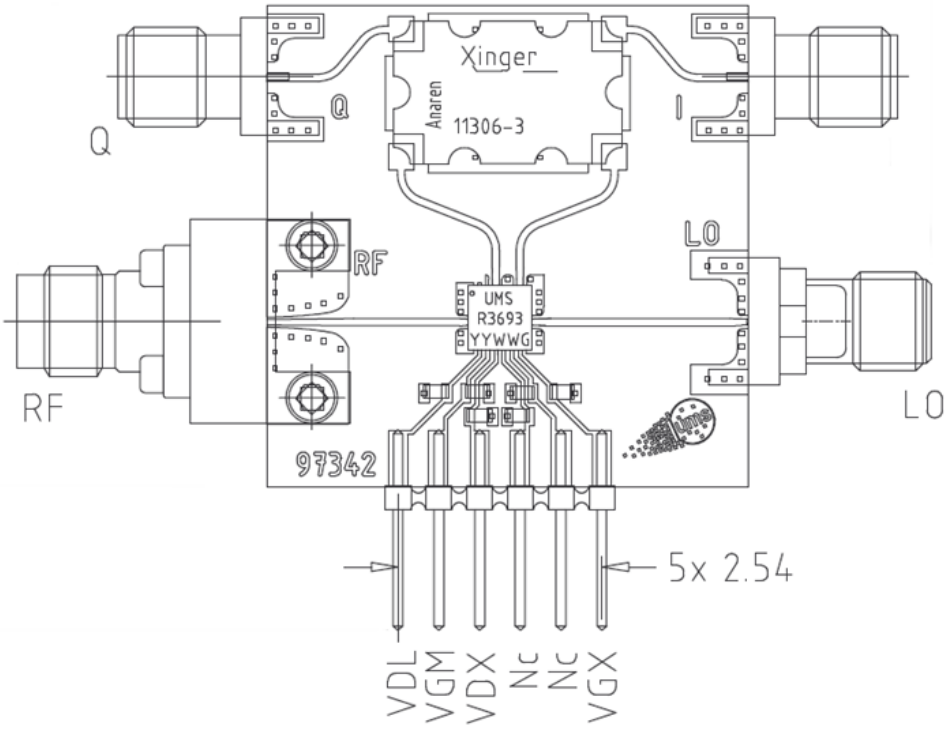
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



10nF capacitor 0603
Hybrid coupler 90° (ex. Anaren 11306-3)

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Note

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 RoHS compliant package:	CHR3693-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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