Low Distortion, High Speed Rail-to-Rail Input/Output Amplifier

Known Good Die

ADA4897-2-KGD

FEATURES

High speed
230 MHz, −3 dB bandwidth (G = +1)
120 V/µs slew rate
Low distortion
−93 dBc at 1 MHz SFDR
−61 dBc at 5 MHz SFDR
Low noise
1 nV/√Hz voltage noise
2.8 pA/√Hz current noise
Low offset voltage: 500 µV maximum
Low power: 3.2 mA/amplifier supply current maximum
Disable mode
Wide supply range: 3 V to 10 V
Known good die (KGD): these die are fully guaranteed to data sheet specifications

APPLICATIONS

Low noise preamplifiers
Ultrasound amplifiers
PLL loop filters
Active filters
ADC drivers
Low voltage instrumentation
DAC buffers

GENERAL DESCRIPTION

The ADA4897-2-KGD[1] is a high speed amplifier with rail-to-rail input and output that operates on low supply voltages and is optimized for high performance and a wide dynamic signal range. The ADA4897-2-KGD has low noise (1 nV/√Hz, 2.8 pA/√Hz) and low distortion (−93 dBc at 1 MHz). In applications that use a fraction of or the entire input dynamic range and require low distortion, the ADA4897-2-KGD is an ideal choice.

Many rail-to-rail input amplifiers have an input stage that switches from one differential pair to another as the input signal crosses a threshold voltage, which causes distortion. The ADA4897-2-KGD has a unique feature that allows the user to select the input crossover threshold voltage through the $\overline{\text{DISABLE}}$x pin. This feature controls the voltage at which the complementary transistor input pairs switch. The ADA4897-2-KGD also has intrinsically low crossover distortion. With its wide supply voltage range (3 V to 10 V) and wide bandwidth (230 MHz), the ADA4897-2-KGD amplifier is designed to work in a variety of applications where speed and performance are needed on low supply voltages. The ADA4897-2-KGD has a disable mode that is controlled via the $\overline{\text{DISABLE}}$x pin.

The ADA4897-2-KGD is rated to work over the industrial temperature range of −40°C to +125°C.

Additional application and technical information can be found in the ADA4897-2 data sheet.

[1] Protected by U.S. Patent Numbers 6,486,737B1 and 6,518,842B1.

Rev. B **Document Feedback**

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REVISION HISTORY

3/15—Rev. A to Rev. B

Changes to Figure 1 and Table 5 9
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Update Outline Dimensions 10
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11/14—Rev. 0 to Rev. A

Change to Thickness Parameter, Table 6 10

4/14—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

T_A = 25°C, G = +1, R_L = 1 kΩ to ground, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		230		MHz
	G = +1, V_{OUT} = 2 V p-p		30		MHz
	G = +2, V_{OUT} = 0.02 V p-p		90		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p, R_L = 100 Ω		7		MHz
Slew Rate	G = +2, V_{OUT} = 6 V step		120		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		45		ns
Settling Time to 0.01%	G = +2, V_{OUT} = 2 V step		90		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (SFDR)	V_{OUT} = 2 V p-p				
	f_C = 100 kHz		−115		dBc
	f_C = 1 MHz		−93		dBc
	f_C = 2 MHz		−80		dBc
	f_C = 5 MHz		−61		dBc
Input Voltage Noise	f = 10 Hz		2.4		nV/√Hz
	f = 100 kHz		1		nV/√Hz
Input Current Noise	f = 10 Hz		11		pA/√Hz
	f = 100 kHz		2.8		pA/√Hz
0.1 Hz to 10 Hz Noise	G = +101, R_F = 1 kΩ, R_G = 10 Ω		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		−500	−28	+500	µV
Input Offset Voltage Drift			0.2		µV/°C
Input Bias Current		−17	−11	−4	µA
Input Bias Current Drift			3		nA/°C
Input Bias Offset Current		−0.6	−0.02	+0.6	µA
Open-Loop Gain	V_{OUT} = −4 V to +4 V	100	110		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common-Mode			10		MΩ
Differential			10		kΩ
Input Capacitance					
Common-Mode			3		pF
Differential			11		pF
Input Common-Mode Voltage Range			−4.9 to +4.1		V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = −2 V to +2 V	−92	−120		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = ±5 V, G = +2		81		ns
Output Voltage Swing					
Positive	R_L = 1 kΩ	4.85	4.96		V
	R_L = 100 Ω	4.5	4.73		V
Negative	R_L = 1 kΩ	−4.85	−4.97		V
	R_L = 100 Ω	−4.5	−4.84		V
Output Current	SFDR = −45 dBc		80		mA
Short-Circuit Current	Sinking/sourcing		135		mA
Capacitive Load Drive	30% overshoot, G = +2		39		pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier		2.8	3.0	3.2	mA
	$\overline{\text{DISABLEx}}$ = −5 V		0.13	0.25	mA
Power Supply Rejection Ratio (PSRR)					
Positive	$+V_S$ = 4 V to 6 V, $-V_S$ = −5 V	−96	−125		dB
Negative	$+V_S$ = 5 V, $-V_S$ = −4 V to −6 V	−96	−121		dB
$\overline{\text{DISABLEx}}$ PIN					
$\overline{\text{DISABLEx}}$ Voltage	Enabled		>$+V_S$ − 0.5		V
	Disabled		<$+V_S$ − 2		V
Input Current					
Enabled	$\overline{\text{DISABLEx}}$ = +5 V		−1.2		µA
Disabled	$\overline{\text{DISABLEx}}$ = −5 V		−40		µA
Switching Speed					
Enabled			0.25		µs
Disabled			12		µs

+5 V SUPPLY

T_A = 25°C, G = +1, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		230		MHz
	G = +1, V_{OUT} = 2 V p-p		30		MHz
	G = +2, V_{OUT} = 0.02 V p-p		90		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p, R_L = 100 Ω		7		MHz
Slew Rate	G = +2, V_{OUT} = 3 V step		100		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		45		ns
Settling Time to 0.01%	G = +2, V_{OUT} = 2 V step		95		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (SFDR)	V_{OUT} = 2 V p-p				
	f_C = 100 kHz		−115		dBc
	f_C = 1 MHz		−93		dBc
	f_C = 2 MHz		−80		dBc
	f_C = 5 MHz		−61		dBc
Input Voltage Noise	f = 10 Hz		2.4		nV/√Hz
	f = 100 kHz		1		nV/√Hz
Input Current Noise	f = 10 Hz		11		pA/√Hz
	f = 100 kHz		2.8		pA/√Hz
0.1 Hz to 10 Hz Noise	G = +101, R_F = 1 kΩ, R_G = 10 Ω		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		−500	−30	+500	µV
Input Offset Voltage Drift			0.2		µV/°C
Input Bias Current		−17	−11	−4	µA
Input Bias Current Drift			3		nA/°C
Input Bias Offset Current		−0.6	−0.02	+0.6	µA
Open-Loop Gain	V_{OUT} = 0.5 V to 4.5 V	97	110		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Resistance					
Common-Mode			10		MΩ
Differential			10		kΩ
Input Capacitance					
Common-Mode			3		pF
Differential			11		pF
Input Common-Mode Voltage Range			0.1 to 4.1		V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 1 V to 4 V	−91	−118		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = 0 V to 5 V, G = +2		96		ns
Output Voltage Swing					
Positive	R_L = 1 kΩ	4.85	4.98		V
	R_L = 100 Ω	4.8	4.88		V
Negative	R_L = 1 kΩ	0.15	0.014		V
	R_L = 100 Ω	0.2	0.08		V
Output Current	SFDR = −45 dBc		70		mA
Short-Circuit Current	Sinking/sourcing		125		mA
Capacitive Load Drive	30% overshoot, G = +2		39		pF
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier		2.6	2.8	2.9	mA
	$\overline{\text{DISABLE}}$x = 0 V		0.05	0.18	mA
Power Supply Rejection Ratio (PSRR)					
Positive	$+V_S$ = 4.5 V to 5.5 V, $-V_S$ = 0 V	−96	−123		dB
Negative	$+V_S$ = 5 V, $-V_S$ = −0.5 V to +0.5 V	−96	−121		dB
$\overline{\text{DISABLE}}$x PIN					
$\overline{\text{DISABLE}}$x Voltage	Enabled		>$+V_S$ − 0.5		V
	Disabled		<$+V_S$ − 2		V
Input Current					
Enabled	$\overline{\text{DISABLE}}$x = 5 V		−1.2		µA
Disabled	$\overline{\text{DISABLE}}$x = 0 V		−20		µA
Switching Speed					
Enabled			0.25		µs
Disabled			12		µs

+3 V SUPPLY

T_A = 25°C, G = +1, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		230		MHz
	G = −1, V_{OUT} = 1 V p-p		45		MHz
	G = +2, V_{OUT} = 0.02 V p-p		90		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p, R_L = 100 Ω		7		MHz
Slew Rate	G = +2, V_{OUT} = 1 V step		85		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		45		ns
Settling Time to 0.01%	G = +2, V_{OUT} = 2 V step		96		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion (SFDR)	f_C = 100 kHz, V_{OUT} = 2 V p-p, G = +2		−105		dBc
	f_C = 1 MHz, V_{OUT} = 1 V p-p, G = −1		−84		dBc
	f_C = 2 MHz, V_{OUT} = 1 V p-p, G = −1		−77		dBc
	f_C = 5 MHz, V_{OUT} = 1 V p-p, G = −1		−60		dBc
Input Voltage Noise	f = 10 Hz		2.3		nV/√Hz
	f = 100 kHz		1		nV/√Hz
Input Current Noise	f = 10 Hz		11		pA/√Hz
	f = 100 kHz		2.8		pA/√Hz
0.1 Hz to 10 Hz Noise	G = +101, R_F = 1 kΩ, R_G = 10 Ω		99		nV p-p
DC PERFORMANCE					
Input Offset Voltage		−500	−30	+500	µV
Input Offset Voltage Drift			0.2		µV/°C
Input Bias Current		−17	−11	−4	µA
Input Bias Current Drift			3		nA/°C
Input Bias Offset Current		−0.6	−0.02	+0.6	µA
Open-Loop Gain	V_{OUT} = 0.5 V to 2.5 V	95	108		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common-Mode			10		MΩ
Differential			10		kΩ
Input Capacitance					
Common-Mode			3		pF
Differential			11		pF
Input Common-Mode Voltage Range			0.1 to 2.1		V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 1.1 V to 1.9 V	−90	−124		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = 0 V to 3 V, G = +2		83		ns
Output Voltage Swing					
Positive	R_L = 1 kΩ	2.85	2.97		V
	R_L = 100 Ω	2.8	2.92		V
Negative	R_L = 1 kΩ	0.15	0.01		V
	R_L = 100 Ω	0.2	0.05		V
Output Current	SFDR = −45 dBc		60		mA
Short-Circuit Current	Sinking/sourcing		120		mA
Capacitive Load Drive	30% overshoot, G = +2		39		pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			3 to 10		V
Quiescent Current per Amplifier		2.5	2.7	2.9	mA
	$\overline{\text{DISABLE}}x$ = 0 V		0.035	0.15	mA
Power Supply Rejection Ratio (PSRR)					
Positive	$+V_S$ = 2.7 V to 3.7 V, $-V_S$ = 0 V	−96	−121		dB
Negative	$+V_S$ = 3 V, $-V_S$ = −0.3 V to +0.7 V	−96	−120		dB
$\overline{\text{DISABLE}}x$ PIN					
$\overline{\text{DISABLE}}x$ Voltage	Enabled		>$+V_S$ − 0.5		V
	Disabled		<$-V_S$ + 2		V
Input Current					
Enabled	$\overline{\text{DISABLE}}x$ = 3 V		−1.2		µA
Disabled	$\overline{\text{DISABLE}}x$ = 0 V		−15		µA
Switching Speed					
Enabled			0.25		µs
Disabled			12		µs

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12.6 V
Common-Mode Input Voltage	$\pm V_S \pm 0.5$ V
Differential Input Voltage	±1.8 V
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +125°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

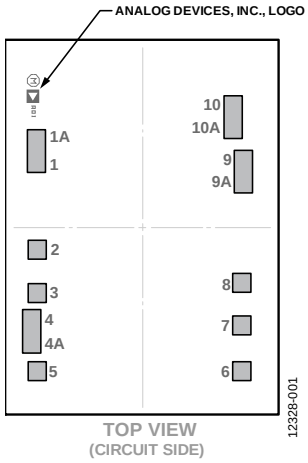

Figure 1. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	X-Axis	Y-Axis	Mnemonic	Description
1	−402	+279	OUT1	Output 1
1A	−402	+354	OUT1	Output 1, Double Bond Pad
2	−400	−41	−IN1	Inverting Input 1
3	−400	−197	+IN1	Noninverting Input 1
4	−420	−303	$-V_S$	Negative Supply
4A	−420	−378	$-V_S$	Negative Supply, Double Bond Pad
5	−395	−485	$\overline{\text{DISABLE1}}$	Disable Control 1
6	+395	−485	$\overline{\text{DISABLE2}}$	Disable Control 2
7	+402	−317	+IN2	Noninverting Input 2
8	+402	−161	−IN2	Inverting Input 2
9	+402	+275	OUT2	Output 2
9A	+402	+203	OUT2	Output 2, Double Bond Pad
10	+364	+477	$+V_S$	Positive Supply
10A	+364	+402	$+V_S$	Positive Supply, Double Bond Pad

OUTLINE DIMENSIONS

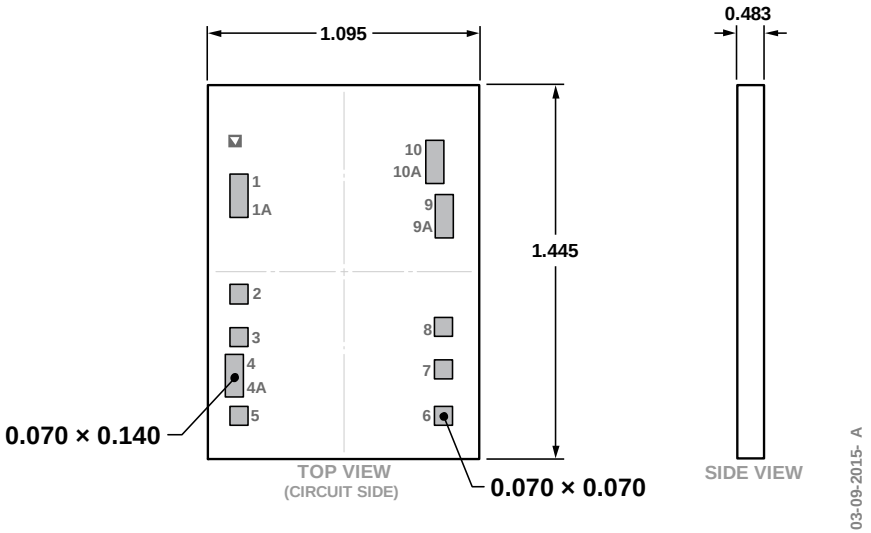

Figure 2. 10-Pad Bare Die [CHIP]
(C-10-6)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Die Specifications

Parameter	Value	Unit
Scribe Line Width	75	µm
Die Size (Maximum Size)	1095 × 1445	µm
Thickness	483	µm
Bond Pads (Minimum Size)	70 × 70	µm
Bond Pad Composition	1% AlCu	%
Backside	Si	Not applicable
Passivation	Doped oxide/SiN	Not applicable
ESD	HBM 2000	V

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Ablestik 84-1LMIS R4
Bonding Method	1 mil gold

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADA4897-2-KGD	–40°C to +125°C	10-Pad Bare Die [CHIP]	C-10-6