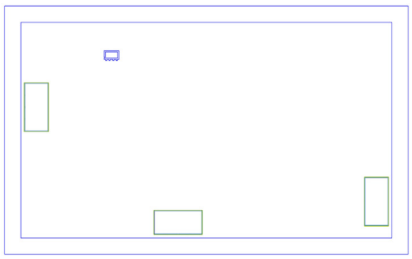
Ultra Flat Gain, Low Noise/High Dynamic Range

Monolithic Amplifier Die

PGA-105-D+

50Ω 0.04 to 2.6 GHz



The Big Deal

- Ultra Flat Gain
- Low Noise, High Dynamic Range
- Excellent Input and Output Return Loss without use of external matching components

Product Overview

PGA-105-D+ (RoHS compliant) is an advanced ultra flat gain amplifier die fabricated using E-PHEMT technology and offers extremely high dynamic range over a broad frequency range and with low noise figure. In addition, the PGA-105-D+ has good input and output return loss over a broad frequency range without the need for external matching components.

Key Features

Feature	Advantages
Broad Band: 0.04 to 2.6 GHz	Broadband covering primary wireless communications bands: Cellular, PCS, LTE, WiMAX
Ultra Flat Gain: ↑ ±0.2 dB typ. 0.1 to 2 GHz	Ideal for use in broad band or multi band applications where gain flatness is critical.
High IP3 Versus DC power Consumption: 37 dBm typical at 0.9 GHz 34 dBm typical at 2 GHz	The PGA-105-D+ provides good IP3 performance relative to device size and power consumption. The combination of the design and E-PHEMT Structure provides enhanced linearity over a broad frequency range as evidence in the IP3 being typically 14 dB above the P 1dB point. This feature makes this amplifier ideal for use in: • Driver amplifiers for complex waveform up converter paths • Drivers in linearized transmit systems • Secondary amplifiers in ultra High Dynamic range receivers
No External Matching Components Required	Unlike competing products, Mini-Circuits PGA-105-D+ provides outstanding gain flatness and Input and Output Return Loss of 23 dB up to 2.6 GHz without the need for any external matching components.
Low Noise Figure: 1.7 - 2.0 dB typ.	A unique feature of the PGA-105-D+ which separates this design from all competitors is the low noise figure performance in combination with the high dynamic range.
Unpackaged Die	Enables users to integrate the amplifier directly into hybrids

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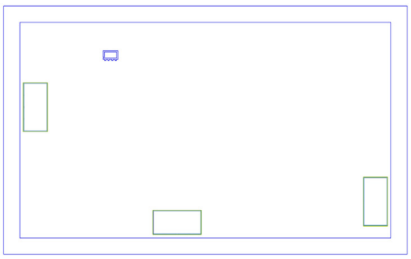


Product Features

- Excellent gain flatness, ±0.2 dB over 0.1-2.0 GHz
- Gain, 15.0 dB typ. at 2 GHz
- High IP3, 37 dBm typ. at 0.9 GHz
- P1dB 18.4 dBm typ. at 2 GHz
- Low noise figure, 1.8 dB at 2 GHz
- No external matching components required

+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Ordering Information: Refer to Last Page

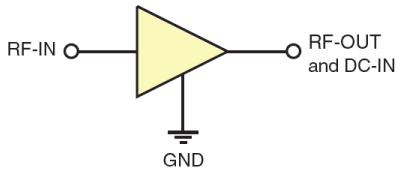
Typical Applications

- Base station infrastructure
- Portable Wireless
- CATV & DBS
- MMDS & Wireless LAN
- LTE

General Description

PGA-105-D+ (RoHS compliant) is an advanced ultra flat gain amplifier fabricated using E-PHEMT technology and offers extremely high dynamic range over a broad frequency range and with low noise figure. In addition, the PGA-105-D+ has good input and output return loss over a broad frequency range without the need for external matching components.

simplified schematic and pin description



Pad	Description
RF-IN	RF input pad. This pad requires the use of an external DC blocking capacitor chosen for the frequency of operation.
RF-OUT and DC-IN	RF output and bias pad. DC voltage is present on this pad; therefore a DC blocking capacitor is necessary for proper operation. An RF choke is needed to feed DC bias without loss of RF signal due to the bias connection, as shown in “Recommended Application Circuit”, Fig. 2
GND	Connections to ground.

Electrical Specifications[1] at 25°C, 50Ω and 5V, unless noted

Parameter	Condition (GHz)	Min.	Typ.	Max.	Units
Frequency range		0.04		2.6	GHz
Gain	0.04 0.5 0.9 2.0 2.6		16.2 14.9 14.9 15.1 15.3		dB
Gain flatness	0.1 - 2.0		±0.2		dB
Noise figure	0.04 0.5 0.9 2.0 2.6		1.5 2.0 1.9 1.8 1.8		
Input return loss	0.04 0.5 0.9 2.0 2.6		11.6 21.6 20.5 25.0 15.3		dB
Output return loss	0.04 0.5 0.9 2.0 2.6		12.6 23.7 22.4 12.5 9.1		dB
Reverse isolation	2.0		21.6		dB
Output power @1dB compression	0.04 0.5 0.9 2.0 2.6		19.8 19.6 19.4 18.4 18.6		dBm
Output IP3	0.04 0.5 0.9 2.0 2.6		33.7 36.6 36.9 33.7 32.2		dBm
Device operating voltage			5.0		V
Device operating current		53	65	77	mA
Device current variation vs voltage			0.016		mA/mV
Thermal resistance, junction-to-ground lead			102		°C/W

1. Measured on Mini-Circuits Die Characterization test board. See Characterization Test Circuit (Fig. 1)

Typical Performance with Application Circuits (Die in industry standard SOT-89 package, See Application Note, AN-60-063)

Frequency (GHz)	TB-678-105+								TB-733-105+ (unconditionally stable)							
	Gain	Noise Figure	Input Return Loss	Output Return Loss	Output Power @ 1dB comp.	Output IP3	Stability Factor	Stability Measure	Gain	Noise Figure	Input Return Loss	Output Return Loss	Output Power @ 1dB comp.	Output IP3	Stability Factor	Stability Measure
0.04	16.4	1.7	11.6	12.9	20.9	36.1	0.93	0.59	14.4	2.3	8.6	27.6	19.5	34.6	1.14	0.90
0.5	15.2	2.0	20.4	23.3	20.7	39.3	1.10	0.62	14.5	2.0	21.8	22.7	21.0	38.7	1.13	0.65
0.9	15.1	1.9	18.4	20.1	20.5	39.3	1.13	0.66	14.4	1.9	20.6	25.1	21.0	37.4	1.17	0.70
2	15.2	1.9	18.9	14.7	19.3	34.7	1.29	0.80	15.5	1.9	13.8	15.2	18.9	33.6	1.35	0.88
2.6	15.9	2.1	9.3	9.1	19.3	32.4	1.51	0.96	15.1	2.0	10.5	8.5	19.4	33.2	1.83	0.94

Absolute Maximum Ratings[2]

Parameter	Ratings
Operating Temperature (ground lead)	-40°C to 85°C
Operating Current at 5.0V	94 mA
Power Dissipation	0.47 W
Input Power (CW)	23 dBm (5 minutes max, 17 dBm (continuous)
DC Voltage on Pad 3	5.5 V

2. Permanent damage may occur if any of these limits are exceeded.
Performance of die measured in industry standard SOT-89 package.
Electrical maximum ratings are not intended for continous normal operation.

Characterization Test Circuit

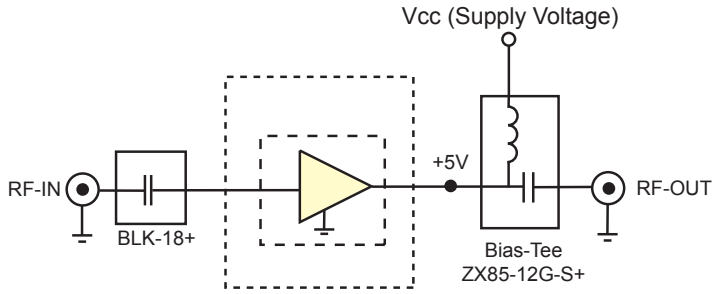
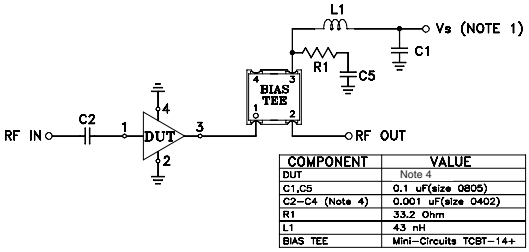


Fig 1. Block Diagram of Test Circuit used for Die characterization.
Gain, Return loss, Output power at 1dB compression (P1 dB) , output IP3 (OIP3) and noise figure measured using Agilent's N5242A PNA-X microwave network analyzer.

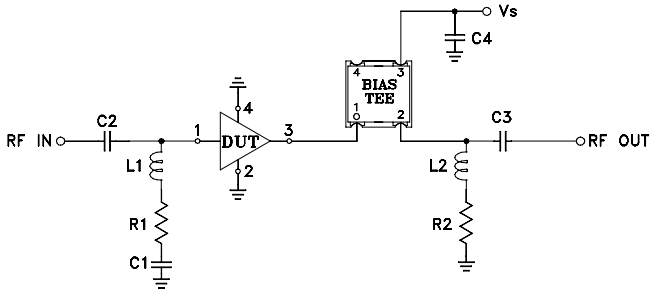
Conditions:
1. Gain and Return loss: Pin= -25dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 0 dBm/tone at output.

Recommended Application Circuits[4]



COMPONENT	VALUE
DUT	Note 4
C1,C5	0.1 uF(size 0805)
C2-C4 (Note 4)	0.001 uF(size 0402)
R1	33.2 Ohm
L1	43 nH
BIAS TEE	Mini-Circuits TCBT-14+

Fig 2. Evaluation board TB-678-105+ includes case, connectors, and components soldered to PCB



COMPONENT	VALUE	SIZE
DUT	Note 4	SOT-89
C1	330 pF	0402
C2,C3	0.001 uF	0402
C4	0.1 uF	0805
R1	422 Ohm	0402
R2	47.5 Ohm	0402
L1, L2	330 nH	0805
BIAS TEE	Mini-Circuits TCBT-14+	

Fig 3. Evaluation board TB-733-105+ with unconditional stability (see applications note AN-60-063)

Die Layout

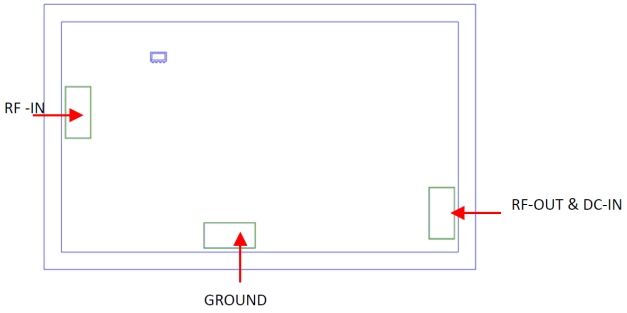
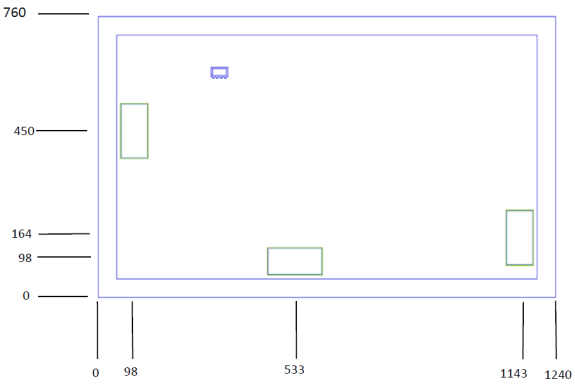


Fig 3. Die Layout

Bonding Pad Position

(Dimensions in µm, Typical)



Critical Dimensions

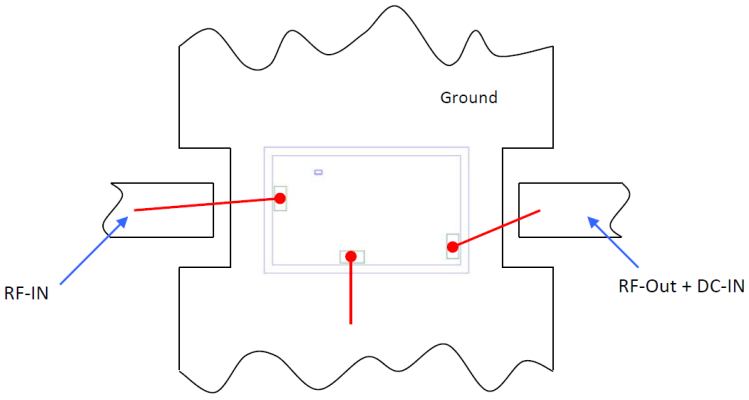
Parameter	Values
Die Thickness, µm	100
Die Width, µm	760
Die Length, µm	1240
Bond Pad Size, µm	150 x 75

[4] Application Circuits bases on die packaged in industry standard SOT-89 package. For reference only.

Assembly and Handling Procedure

1. Storage
   Dice should be stored in a dry nitrogen purged desiccators or equivalent.
2. ESD
   MMIC EPHEMPT amplifier dice are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be opened in clean room conditions at an appropriately grounded anti-static worksta tion. Devices need careful handling using correctly designed collets, vacuum pickup tips or sharp antistatic tweezers to deter ESD damage to dice.
3. Die Attach
   The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are DieMat DM6030HK-PT/H579 or Ablestik 84-1LMISR4. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total die periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. It is recommended to use antistatic die pick up tools only.
4. Wire Bonding
   Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the dice gold bond pads. Thermosonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1 mil diameter. Bonds must be made from the bond pads on the die to the package or substrate. All bond wires should be kept as short as low as reasonable to minimize performance degradation due to undesirable series inductance.

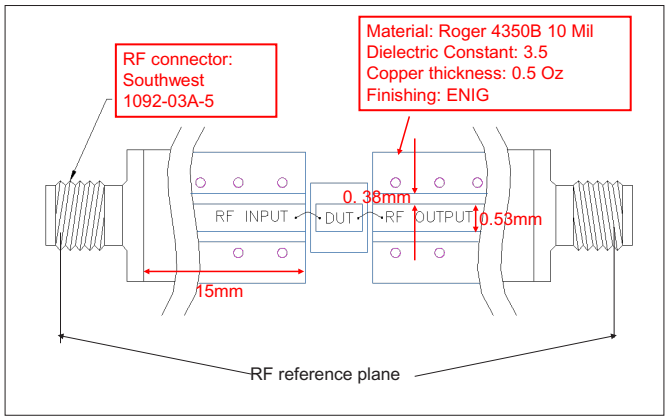
Assembly Diagram



Recommended Wire Length, Typical

Wire	Wire Length (mm)	Wire Loop Height (mm)
RF-IN, RF-OUT + DC-IN	1.0	0.15
GROUND	0.30	0.15

RF Reference Plane - No port extension



Additional Detailed Technical Information *additional information is available on our dash board.*	
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set with and without port extension(.zip file)
Case Style	Die
Die Ordering and packaging information	Quantity, Package — Model No. Small, Gel - Pak: 10,50,100 KGD* — PGA-105-DG+ Medium†, Partial wafer: KGD*<5K — PGA-105-DP+ Large†, Full Wafer — PGA-105-DF+ †*Available upon request contact sales representative* Refer to AN-60-067
Environmental Ratings	ENV-80

*Known Good Dice ("KGD") means that the dice in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such dice fall within a predefined range. While DC testing is not definitive, it does help to provide a higher degree of confidence that dice are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

ESD Rating**

Human Body Model (HBM): Class 1A (250 to <500V) in accordance with ANSI/ESD STM 5.1 - 2001

Machine Model (MM): Class M1(pass 25V) in accordance with ANSI/ESD STM5.2-1999

** Tested in industry standard SOT-89 package.

Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

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