GaAs pHEMT MMIC Low Noise Amplifier, 0.3 GHz to 20 GHz

Data Sheet

HMC1049 Bare Die

FEATURES

Low noise figure: 1.7 dB
High gain: 16 dB
P1dB output power: 15 dBm
Supply voltage: 7 V at 70 mA
Output IP3: 27 dBm
50 Ω matched input/output
Die size: 1.43 mm × 2.9 mm × 0.1 mm

APPLICATIONS

Point-to-point radios
Point-to-multipoint radios
Military and space
Test instrumentation

FUNCTIONAL BLOCK DIAGRAM

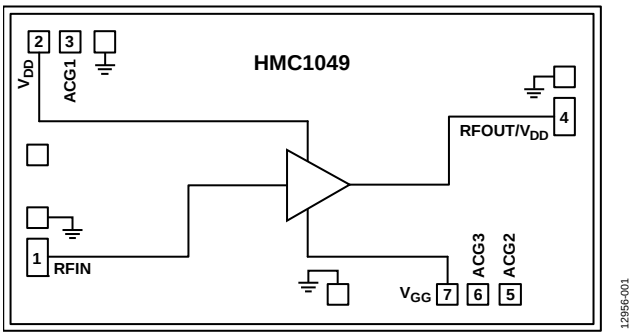

Figure 1.

GENERAL DESCRIPTION

The HMC1049 Bare Die is a GaAs MMIC low noise amplifier (LNA) that operates between 0.3 GHz and 20 GHz. This LNA provides 16 dB of small signal gain, a 1.7 dB noise figure, and an Output IP3 of 27 dBm, requiring only 70 mA from a 7 V supply. The P1dB output power of 16 dBm enables the LNA to function as a local oscillator (LO) driver for balanced, I/Q or image rejection mixers. V_{DD} can be applied to Pad 2 with V_{DD} = 7 V or to Pad 4 with V_{DD} = 4 V. Pad 4 requires a bias tee. The HMC1049 Bare Die is also internally matched to 50 Ω for ease of integration into multichip modules (MCMs). All data is taken with the chip in a 50 Ω test fixture connected via 0.025 mm (1 mil) diameter wire bonds of 0.31 mm (12 mil) length.

Rev. A Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

4/15—Rev. 00.0414 to Rev. A

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Updated Format ..... Universal
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Updated Outline Dimensions 13
Changes to Ordering Guide 13

SPECIFICATIONS

T_A = 25°C, V_{DD} = 7 V, I_{DD} = 70 mA[1].

Table 1.

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
FREQUENCY RANGE	0.3		10	10		16	16		20	GHz
GAIN	12.5	16		12	14.5		11	13		dB
Gain Variation over Temperature		0.012			0.016			0.015		dB/°C
NOISE FIGURE		1.7	2.4		2	2.7		2.7	3.6	dB
RETURN LOSS										
Input		17			14			14		dB
Output		12			17			17		dB
OUTPUT POWER										
Output Power for 1 dB Compression		15			13			12		dBm
Saturated (P_{SAT})		18			16.5			15.5		dBm
Output Third-Order Intercept (IP3)[2]		27			25			23.5		dBm
TOTAL SUPPLY CURRENT (I_{DD}) (V_{DD} = 7 V)		70			70			70		mA

[1] Adjust V_{GG} between −2 V to 0 V to achieve I_{DD} = 70 mA typical.
[2] Measurement taken at P_{OUT}/tone = 4 dBm.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage (V_{DD})	10 V
Drain Bias Voltage (RFOUT/V_{DD})	7 V
RF Input Power	18 dBm
Gate Bias Voltage, V_{GG}	−2 V to +0.2 V
Channel Temperature	175°C
Continuous P_{DISS} (T = 85°C) (Derate 37.4 mW/°C Above 85°C)	3.4 W
Thermal Resistance (Channel to Die Bottom)	26.7°C/W
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

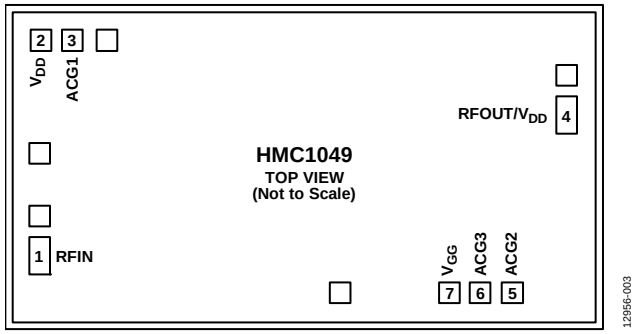


Figure 2. Pad Configuration

Table 3. Pad Function Descriptions

Pad No.	Function	Description
1	RFIN	RF Input. This pad is dc-coupled and matched to 50 Ω.
2	V_{DD}	Power Supply Voltage for the Amplifier. External bypass capacitors are required.
3	ACG1	Low Frequency Termination. Attach an external bypass capacitor (see Figure 34).
4	RFOUT/V_{DD}	RF Output/Alternate Power Supply Voltage for the Amplifier. An external bias tee is required when using Pin 4 as an alternative V_{DD}. This pad is dc-coupled and matched to 50 Ω.
5, 6	ACG2, ACG3	Low Frequency Terminations. Attach external bypass capacitors (see Figure 34).
7	V_{GG}	Gate Control for Amplifier. Adjust to achieve I_{DD} = 70 mA.
Die Bottom	GND	Ground. Die bottom must be connected to RF/dc ground.

INTERFACE SCHEMATICS

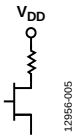


Figure 3. V_{DD} Interface

Figure 4. GND Interface

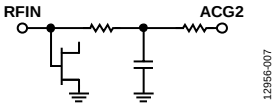


Figure 5. RFIN Interface

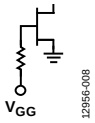


Figure 6. V_{GG} Interface

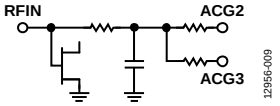


Figure 7. ACG2 and ACG3 Interface

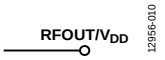


Figure 8. RFOUT/V_{DD} Interface

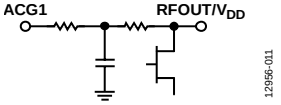


Figure 9. ACG1 Interface

TYPICAL PERFORMANCE CHARACTERISTICS

Data taken with V_{DD} applied to Pad 2, with V_{DD} = 7 V.

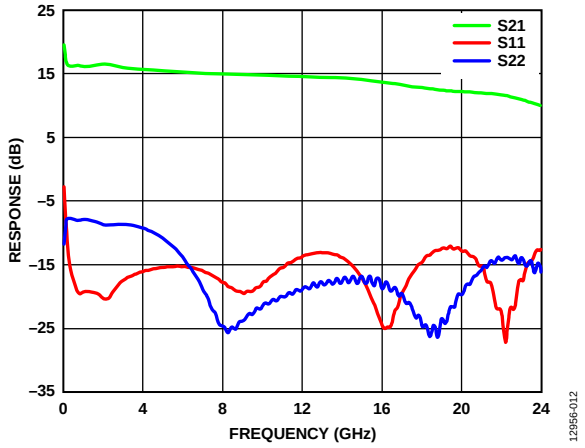


Figure 10. Broadband, Gain, and Return Loss

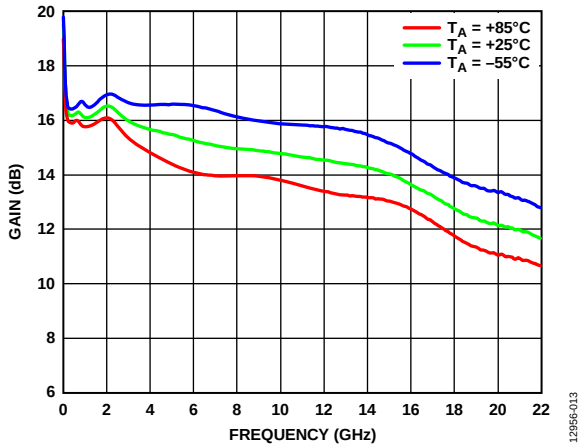


Figure 11. Gain vs. Temperature

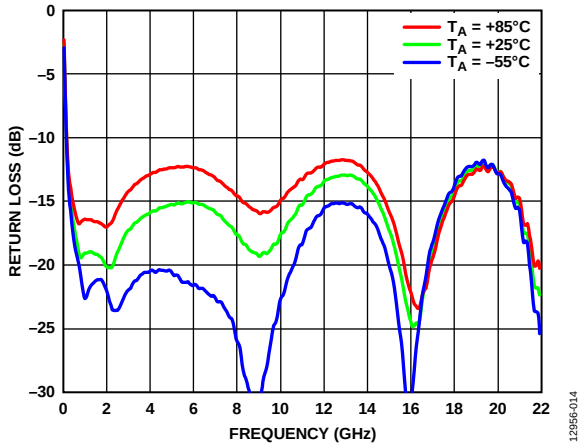


Figure 12. Input Return Loss vs. Temperature

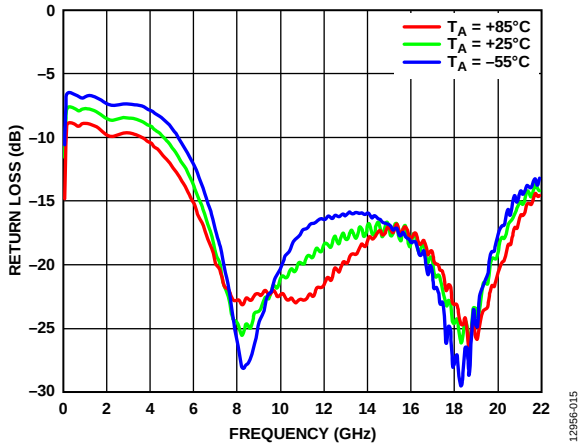


Figure 13. Output Return Loss vs. Temperature

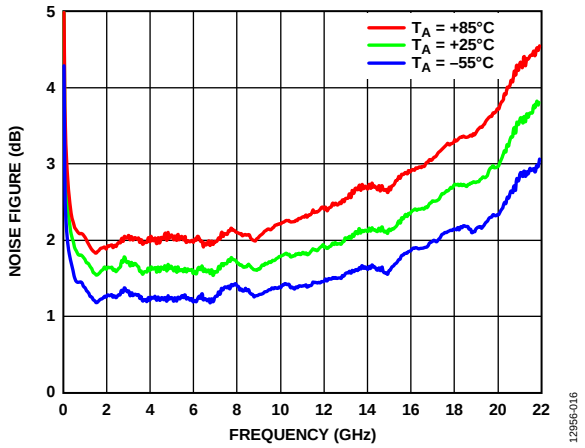


Figure 14. Noise Figure vs. Temperature

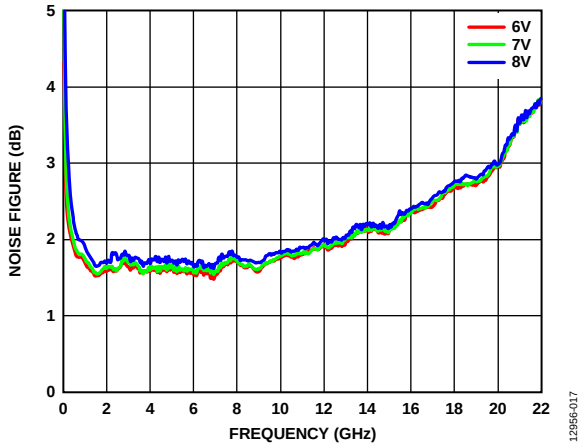


Figure 15. Noise Figure vs. V_{DD}

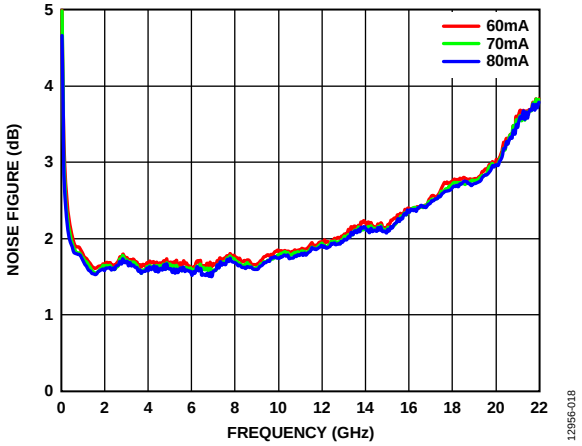


Figure 16. Noise Figure vs. I_{DD}

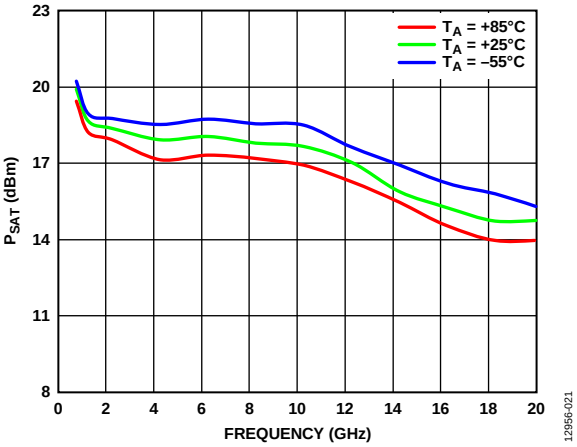


Figure 19. P_{SAT} vs. Temperature

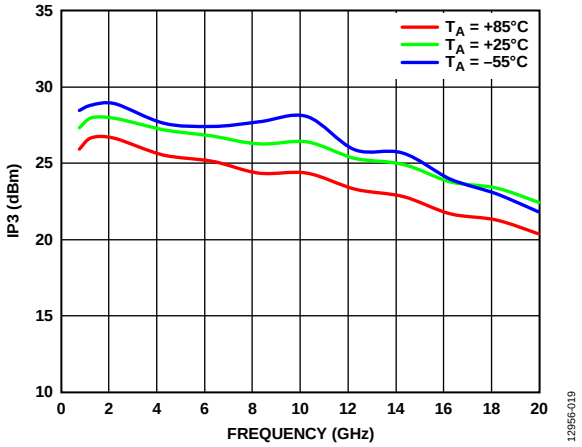


Figure 17. Output IP3 vs. Temperature

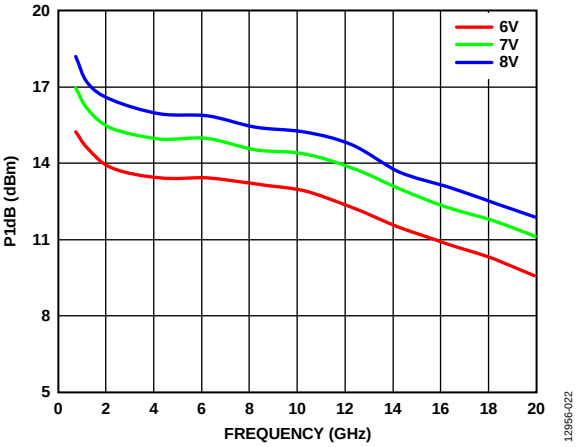


Figure 20. P1dB vs. V_{DD}

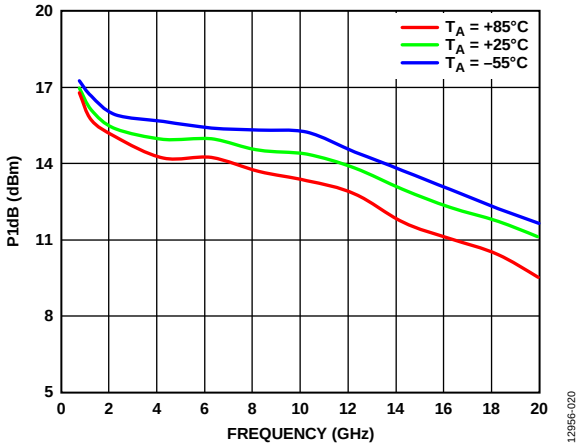


Figure 18. P1dB vs. Temperature

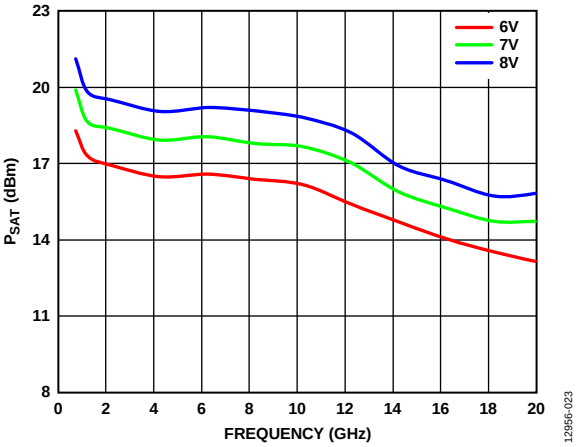


Figure 21. P_{SAT} vs. V_{DD}

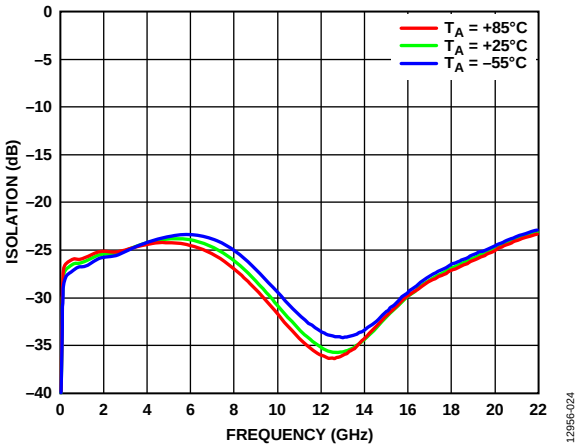


Figure 22. Reverse Isolation vs. Temperature

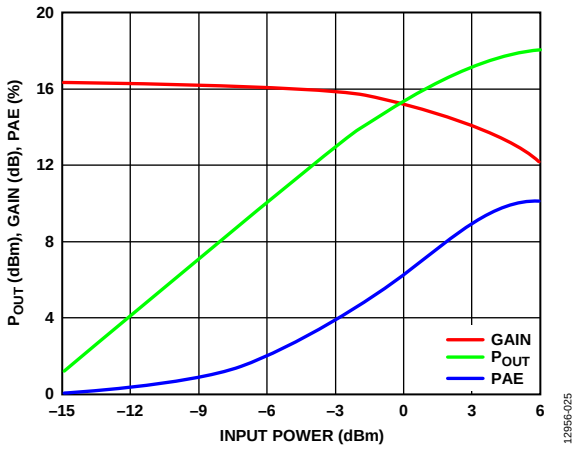


Figure 23. Power Compression at 2 GHz

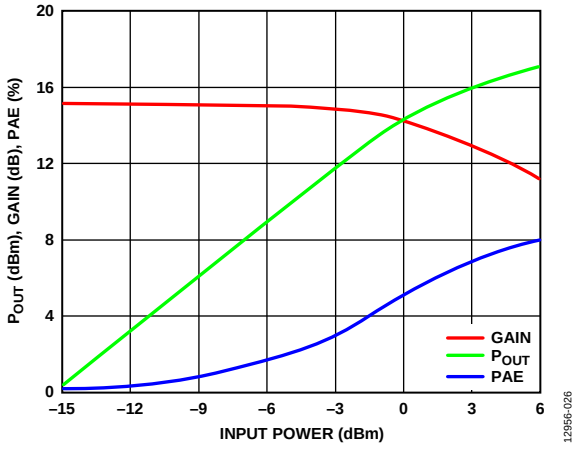


Figure 24. Power Compression at 10 GHz

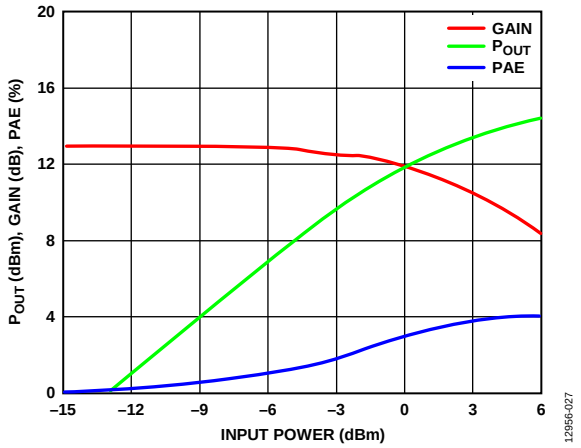


Figure 25. Power Compression at 18 GHz

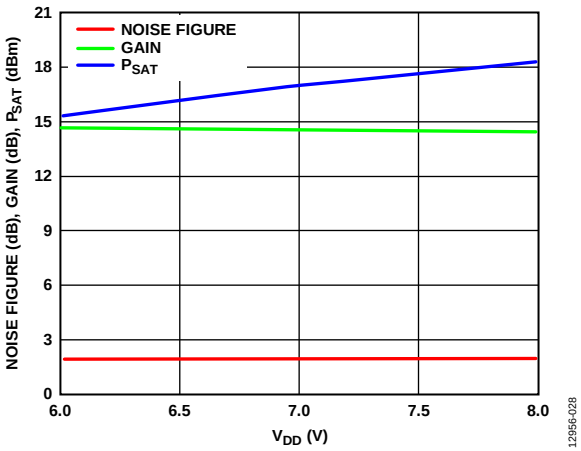


Figure 26. Noise Figure, Gain, and Power (P_{SAT}) vs. Supply Voltage (V_{DD}) at 12 GHz

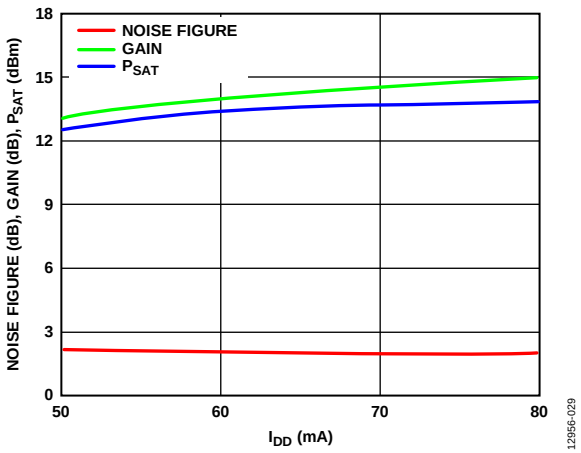


Figure 27. Noise Figure, Gain, and Power vs. Supply Current at 12 GHz

Data taken with V_{DD} = 4 V applied to the bias tee at Pad 4.

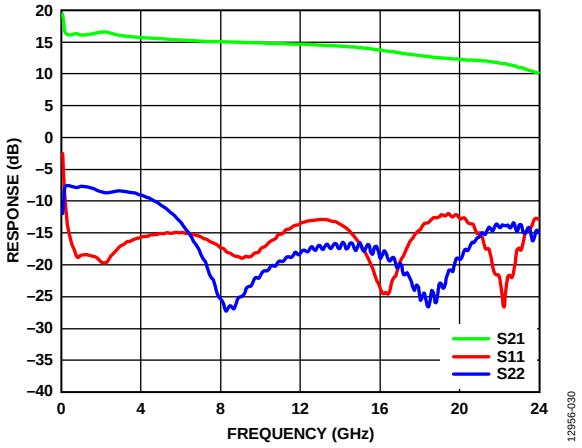


Figure 28. Broadband Gain and Return Loss

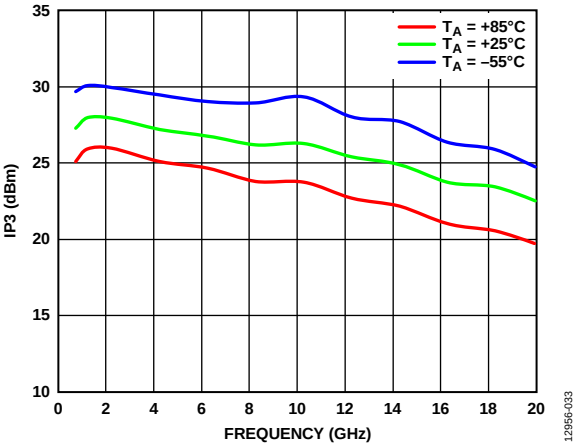


Figure 31. Output IP3 vs. Temperature

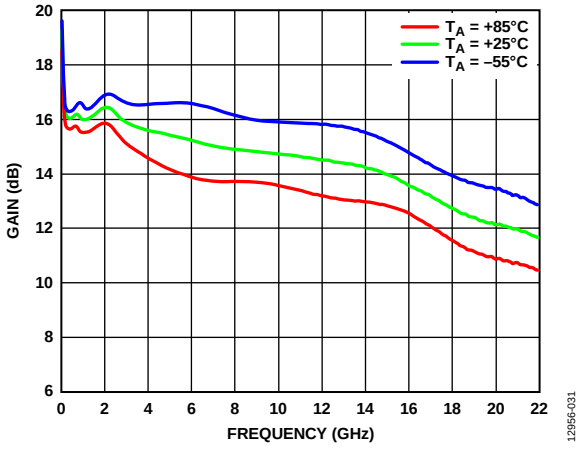


Figure 29. Gain vs. Temperature

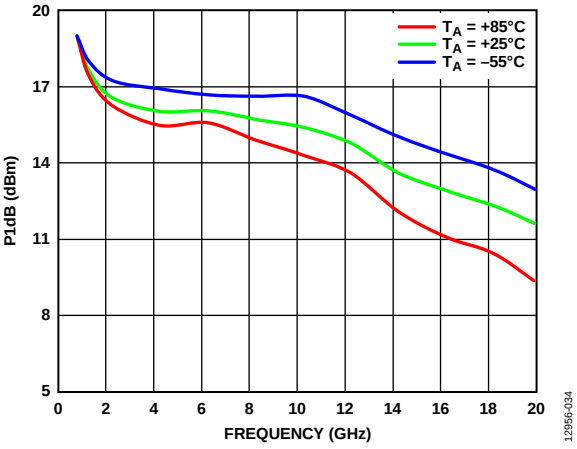


Figure 32. P1dB vs. Temperature

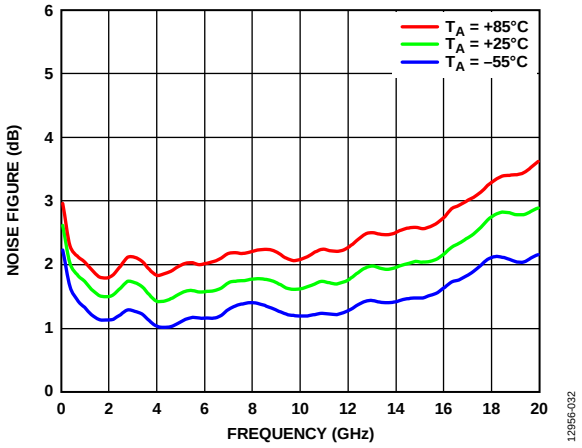


Figure 30. Noise Figure vs. Temperature

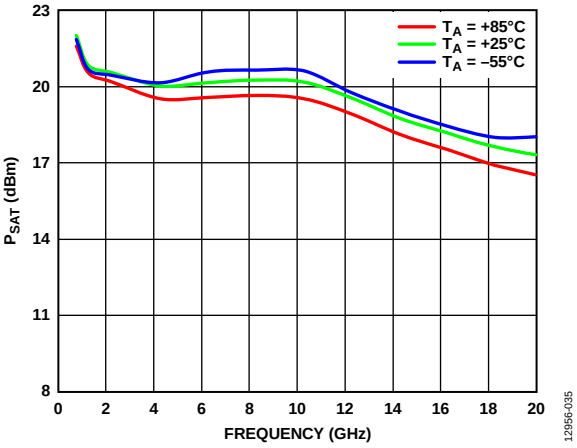


Figure 33. P_{SAT} vs. Temperature

APPLICATION CIRCUIT

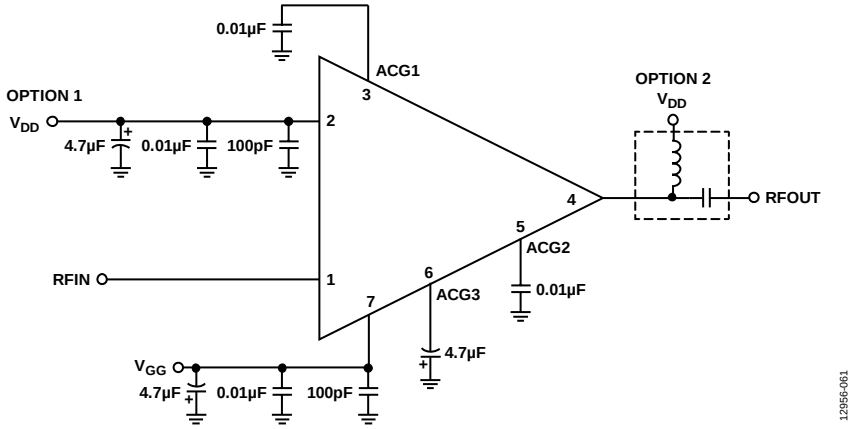


Figure 34. Typical Applications Circuit

ASSEMBLY DIAGRAM

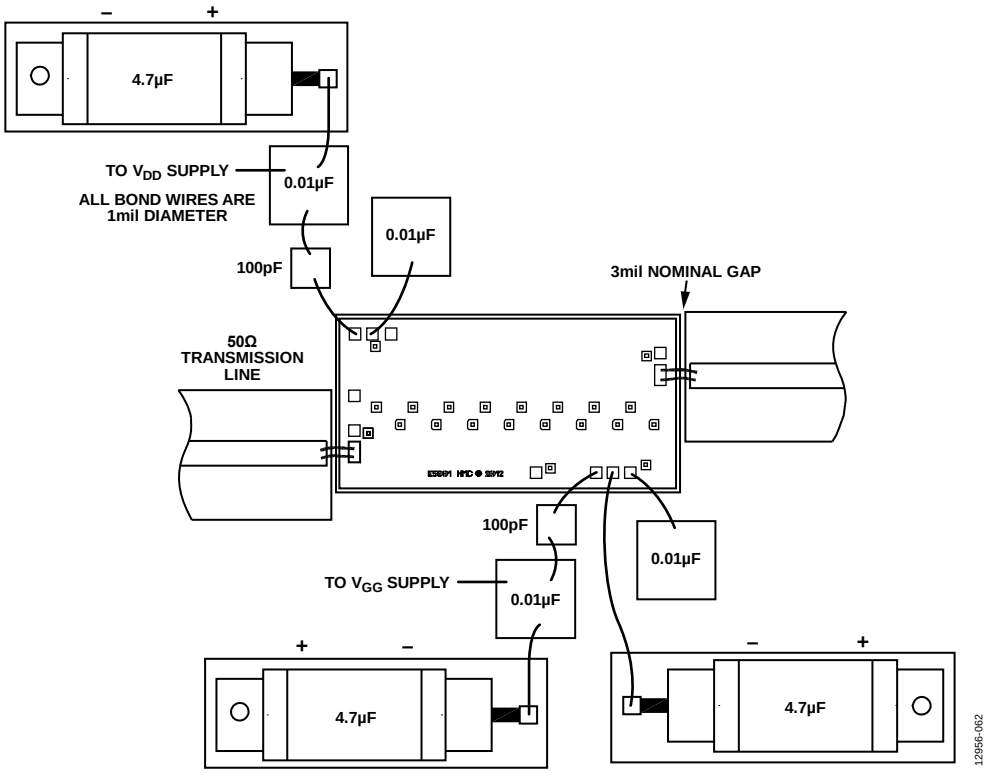


Figure 35. Assembly Diagram

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy.

To bring RF to and from the chip, use 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates (see Figure 36).

If 0.254 mm (10 mil) thick alumina thin film substrates are required, raise the die by 0.150 mm (6 mil) to ensure that the surface of the die is coplanar with the surface of the substrate. One method to accomplish this coplanarity is to attach the 0.102 mm (4 mil) thick die to a 0.150 mm (6 mil) thick molybdenum heat spreader (molytab), and then attach the unit to the ground plane (Figure 37).

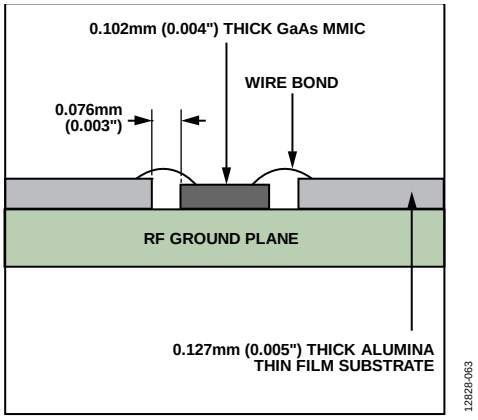


Figure 36. RF Lines

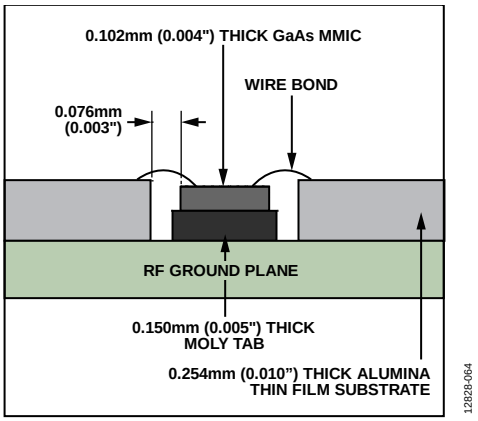


Figure 37. Die Attachment Using Molybdenum Heat Spreader

To minimize bond wire length, place microstrip substrates as close to the die as possible. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

HANDLING PRECAUTIONS

To avoid permanent damage, adhere to the following precautions.

Storage

All bare die ship in either waffle or gel-based ESD protective containers, sealed in an ESD protective bag. After opening the sealed ESD protective bag, all die must be stored in a dry nitrogen environment.

Cleanliness

Handle the chips in a clean environment. Never use liquid cleaning systems to clean the chip.

Static Sensitivity

Follow ESD precautions to protect against ESD strikes.

Transients

Suppress instrument and bias supply transients while bias is applied. To minimize inductive pickup, use shielded signal and bias cables.

General Handling

Handle the chip on the edges only using a vacuum collet or with a sharp pair of bent tweezers. Because the surface of the chip has fragile air bridges, never touch the surface of the chip with a vacuum collet, tweezers, or fingers.

MOUNTING

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach

It is best to use an 80/20 gold tin preform with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90/10 nitrogen/hydrogen gas is applied, maintain tool tip temperature at 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing should be required for attachment.

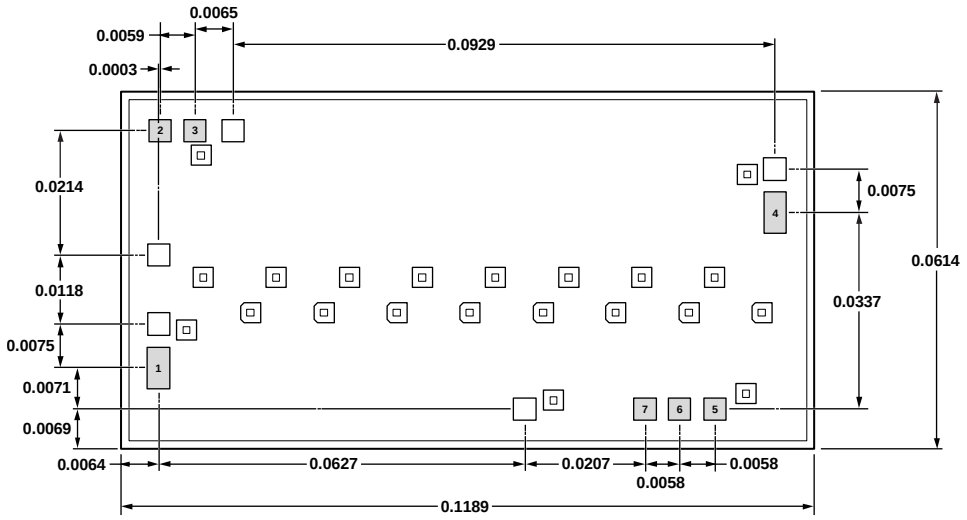
Epoxy Die Attach

Apply a minimum amount of epoxy to the mounting surface so that upon placing it into position, a thin epoxy fillet is observed around the perimeter of the chip. Cure epoxy per the schedule provided by the manufacturer.

WIRE BONDING

RF bonds made with two 1 mil wires are recommended using thermosonic bonding with a force of 40 grams (g) to 60 g. DC bonds of 0.001 in. (0.025 mm) diameter, thermosonically bonded, are recommended. Make ball bonds with a force of 40 g to 50 g and wedge bonds at 18 g to 22 g. Make all bonds with a nominal stage temperature of 150°C. To achieve reliable bonds, apply a minimum amount of ultrasonic energy. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

OUTLINE DIMENSIONS



NOTES:
1. DIE THICKNESS IS 0.004.
2. TYPICAL BOND PAD IS 0.004 SQUARE.
3. BOND PAD METALIZATION: GOLD.
4. BACK SIDE METALIZATION: GOLD.
5. BACK SIDE METAL IS GROUND.
6. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS.
7. OVERALL DIE SIZE IS ±0.002

04-29-2015- A

Figure 38. 7-Pad Bare Die [CHIP]
(C-7-3)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
HMC1049 Bare Die	−55°C to +85°C	7-Pad Bare Die [CHIP]	C-7-3

[1] This is a gel pack option, contact Analog Devices, Inc., for additional packaging options.