High Isolation, Silicon SP4T, Nonreflective Switch, 9 kHz to 12.0 GHz

Preliminary Technical Data

ADRF5040

FEATURES

Nonreflective 50 Ω design
Positive control: 0 V/3.3 V
Low insertion loss: 0.86 dB at 8.0 GHz
High isolation: 35 dB at 8.0 GHz
High power handling
- **33 dBm through path**
- **27 dBm terminated path**

High linearity
- **1 dB compression (P1dB): 37 dBm typical**
- **Input third-order intercept (IIP3): 57 dBm typical**

ESD rating: 4.5 kV human body model (HBM)
4 mm × 4 mm, 24-lead LFCSP package
No low frequency spurious
Settling time (0.05 dB margin of final RF_{OUT}): 9 µs

APPLICATIONS

Test instrumentation
Microwave radios and very small aperture terminals (VSATs)
Military radios, radars, and electronic counter measures (ECMs)
Fiber optics and broadband telecommunications

FUNCTIONAL BLOCK DIAGRAM

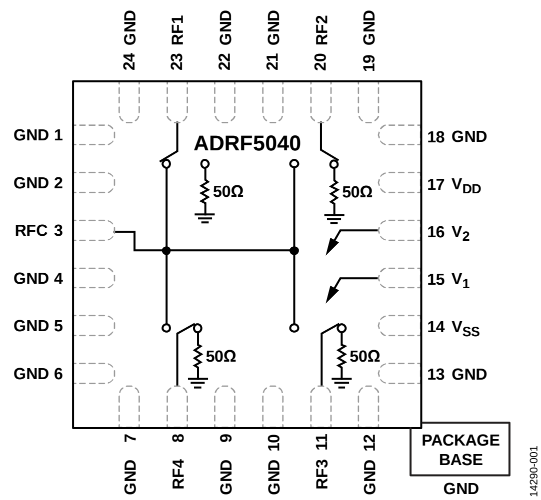

Figure 1.

GENERAL DESCRIPTION

The ADRF5040 is a general-purpose, broadband high isolation, nonreflective single-pole, quad-throw (SP4T) switch in a LFCSP surface mount package. Covering the 9 kHz to 12 GHz range, the switch offers high isolation and low insertion loss. The switch features >34 dB isolation, 0.8 dB insertion loss up to 8.0 GHz, and a 9 µs settling time of 0.05 dB margin of final RF_{OUT}. The switch operates using positive control voltage of +3.3 V and 0 V and requires +3.3 V and −3.3 V supplies. The ADRF5040 is packaged in a 4 mm × 4 mm, surface mount LFCSP package.

Rev. PrB Document Feedback

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Technical Support **www.analog.com**

TABLE OF CONTENTS

Features ... 1
Applications ... 1
Functional Block Diagram ... 1
General Description ... 1
Specifications ... 3
  Electrical Specifications ... 3
  Digital Control Voltages ... 4
  Bias and Supply Current ... 4
Absolute Maximum Ratings ... 5
  ESD Caution ... 5
Pin Configuration and Function Descriptions ... 6
  Interface Schematics ... 7
Typical Performance Characteristics ... 8
  Insertion Loss, Return Loss, and Isolation ... 8
  Insertion Loss, Return Loss, and Isolation ... 9
  Input Power Compression and Input Third-Order Intercept ... 10
  Input Power Compression and Input Third-Order Intercept (10 kHz to 1 GHz) ... 11
Theory of Operation ... 12
Applications Information ... 13
  Evaluation PCB ... 13
Outline Dimensions ... 14

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = -3.3 V, V_1 and V_2 = 0 V/V_{DD}, T_A = 25°C, 50 Ω system, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INSERTION LOSS					
	9 kHz to 4.0 GHz		0.7		dB
	9 kHz to 8.0 GHz		0.8		dB
	9 kHz to 10.0 GHz		1.1		dB
	9 kHz to 12.0 GHz		2		dB
ISOLATION, RFC TO RF1 to RF4 (WORST CASE)					
	9 kHz to 4.0 GHz		44		dB
	9 kHz to 8.0 GHz		34		dB
	9 kHz to 10.0 GHz		29.2		dB
	9 kHz to 12.0 GHz		20		dB
RETURN LOSS					
On State	9 kHz to 4.0 GHz		21		dB
	9 kHz to 8.0 GHz		19		dB
	9 kHz to 10.0 GHz		13.5		dB
	9 kHz to 12.0 GHz		8		dB
Off State	9 kHz to 4.0 GHz		25		dB
	9 kHz to 8.0 GHz		18.6		dB
	9 kHz to 10.0 GHz		15.5		dB
	9 kHz to 12.0 GHz		14.5		dB
RF SETTLING TIME					
	50% V_1/ V_2 to 0.05 dB margin of final RF_{OUT}		9		µs
	50% V_1/ V_2 to 0.1 dB margin of final RF_{OUT}		7		µs
SWITCHING SPEED					
t_{RISE}/t_{FALL}	10% to 90% RF_{OUT}		1.3		µs
t_{ON}/t_{OFF}	50% V_1/V_2 to 90%/10% RF		3.5		µs
INPUT POWER	9 kHz to 12.0 GHz				
1 dB Compression (P1dB)			37		dBm
0.1 dB Compression (P0.1dB)			34		dBm
INPUT THIRD-ORDER INTERCEPT (IIP3)	Two-tone input power = 14 dBm at each tone				
	1 MHz to 2.0 GHz		62		dBm
	1 MHz to 8.0 GHz		58		dBm
	1 MHz to 12.0 GHz		53		dBm
RECOMMENDED OPERATING CONDITIONS					
Positive Supply Voltage (V_{DD})		3.0		3.6	V
Negative Supply Voltage (V_{SS})		−3.6		−3.0	V
Control Voltage (V_1, V_2) Range		0		V_{DD}	V
RF Input Power	V_{DD} = 3.3 V, V_{SS} = −3.3 V, T_A = 85°C, frequency = 2 GHz				
Through Path				33	dBm
Termination Path				27	dBm
Hot Switch Power Level	V_{DD} = 3.3 V, T_A = 85°C, frequency = 2 GHz			27	dBm
Case Temperature Range (T_{CASE})		−40		+85	°C

DIGITAL CONTROL VOLTAGES

V_{DD} = 3.3 V ± 10%, V_{SS} = −3.3 V ± 10%, T_{CASE} = −40°C to +85°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition/Comments
INPUT CONTROL VOLTAGE						<1 µA typical
Low (V_{IL})	V_{IL}	0		0.8	V	
High (V_{IH})	V_{IH}	1.4		V_{DD} + 0.3	V	

BIAS AND SUPPLY CURRENT

T_{CASE} = −40°C to +85°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
SUPPLY CURRENT					
V_{DD} = 3.3 V	I_{DD}		20	100	µA
V_{SS} = −3.3 V	I_{SS}		20	100	µA

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Positive Supply Voltage (V_{DD}) Range	−0.3 V to +3.7 V dc
Negative Supply Voltage (V_{SS}) Range	−3.7 V to +0.3 V
Control Voltage (V_1, V_2) Range	−0.3 V to V_{DD} +0.3 V
RF Input Power[1] (V_{DD}/ V_1, V_2 = 3.3 V, V_{SS} = −3.3 V, T_A = 85°C, Frequency = 2 GHz)	
Through Path	34 dBm
Termination Path	28 dBm
Hot Switch Power Level (V_{DD} = 3.3 V, T_A = 85°C, Frequency = 2 GHz)	30 dBm
Storage Temperature Range	−65°C to +150°C
Channel Temperature	135°C
Thermal Resistance (Channel to Package Bottom)	
Through Path	
Terminated Path	
ESD Sensitivity	
Human Body Model (HBM)	4 kV (Class 3)
Charged Device Model (CDM)	1.25 kV

[1] For recommended operating conditions, see Table 1.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

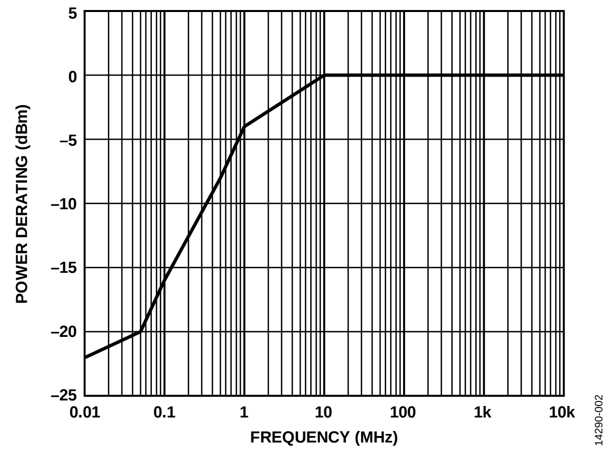


Figure 2. Power Derating Through Path

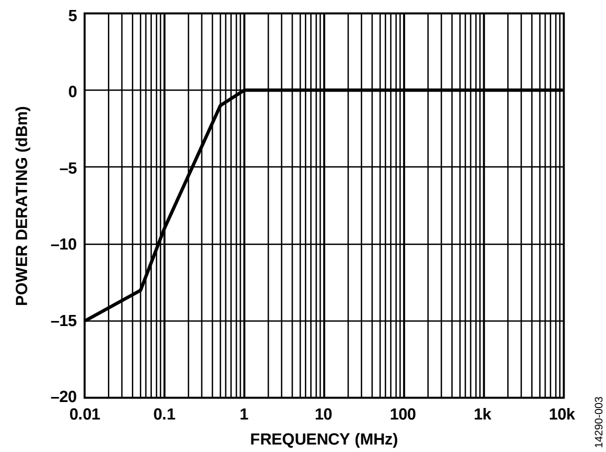


Figure 3. Power Derating Terminated Path

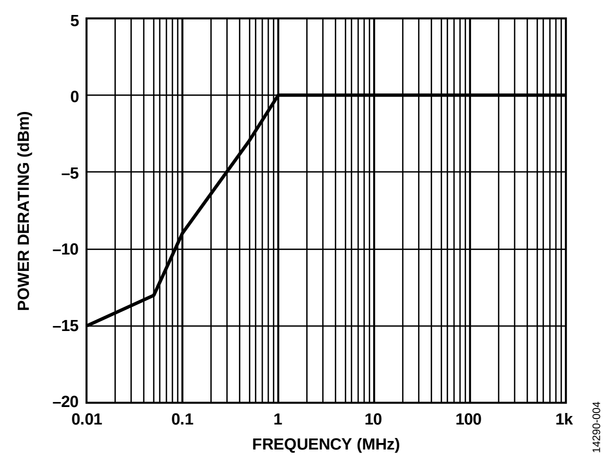
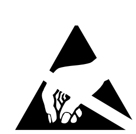


Figure 4. Power Derating for Hot Switching Power

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

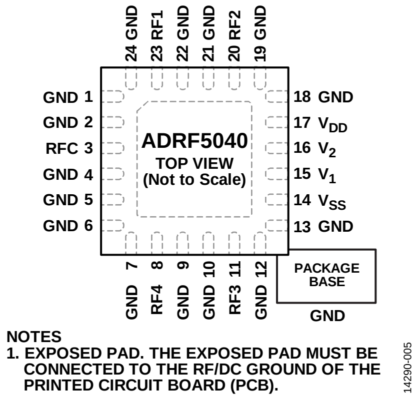


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4 to 7, 9, 10, 12, 13, 18, 19, 21, 22, 24	GND	Ground. The package bottom has an exposed metal pad that must connect to the printed circuit board (PCB) RF ground. See Figure 6 for the GND interface schematic.
3	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if RF line potential is not equal to 0 V dc.
8	RF4	RF4 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if RF line potential is not equal to 0 V dc.
11	RF3	RF3 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if RF line potential is not equal to 0 V dc.
14	V_{SS}	Negative Supply Voltage Pin.
16	V_1	Control Input Pin 1. See Table 2 and Table 6.
15	V_2	Control Input Pin 2. See Table 2 and Table 6.
17	V_{DD}	Positive Supply Voltage PIN.
20	RF2	RF2 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if RF line potential is not equal to 0 V dc.
23	RF1	RF1 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if RF line potential is not equal to 0 V dc.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF /dc ground of the printed circuit board (PCB).

Table 6. Truth Table

Digital Control Inputs		
V_1	**V_2**	**Signal Path State**
Low	Low	RFC to RF1
High	Low	RFC to RF2
Low	High	RFC to RF3
High	High	RFC to RF4

INTERFACE SCHEMATICS

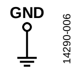


Figure 6. GND Interface Schematic

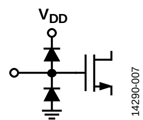


Figure 7. V_2 Interface Schematic

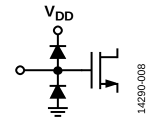


Figure 8. V_1 Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = −3.3 V, T_{CASE} = 25°C, unless otherwise specified.

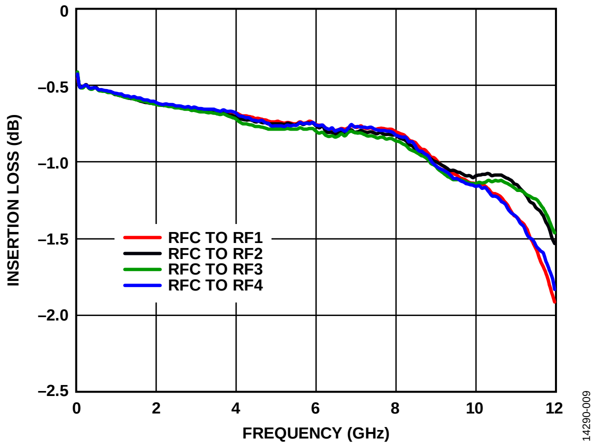


Figure 9. Insertion Loss vs. Frequency

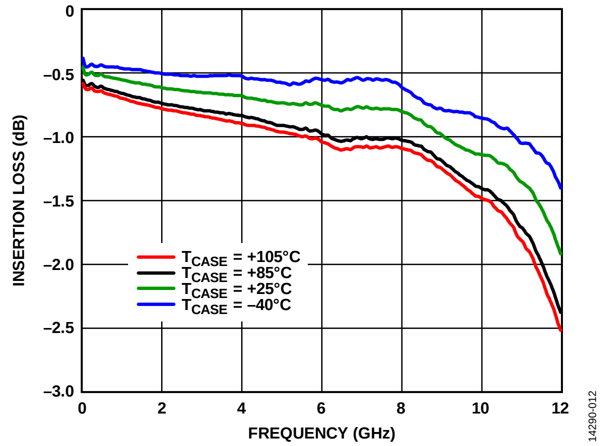


Figure 12. Insertion Loss vs. Frequency RFC to RF1 On or RFC to RF4 On

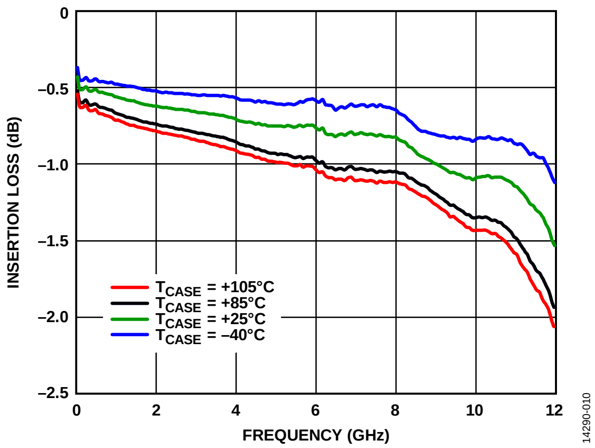


Figure 10. Insertion Loss vs. Frequency RFC to RF2 On or RFC to RF3 On

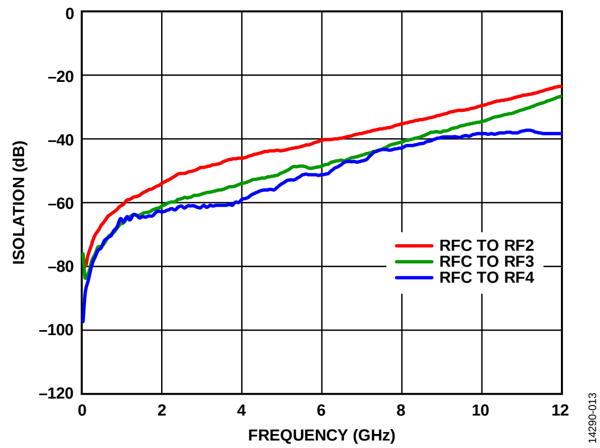


Figure 13. Isolation vs Frequency RFC to RF1 = On

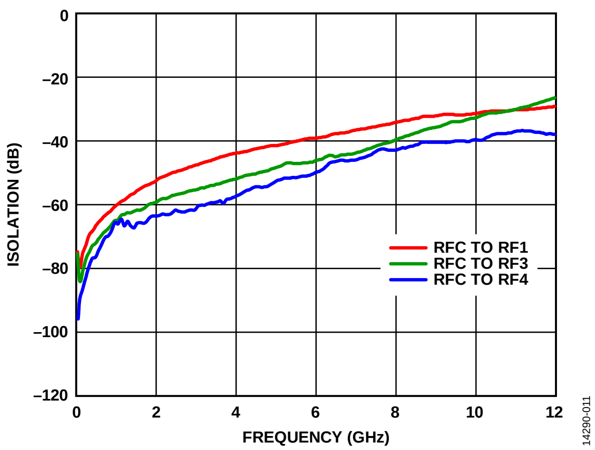


Figure 11. Isolation vs Frequency RFC to RF2 = On

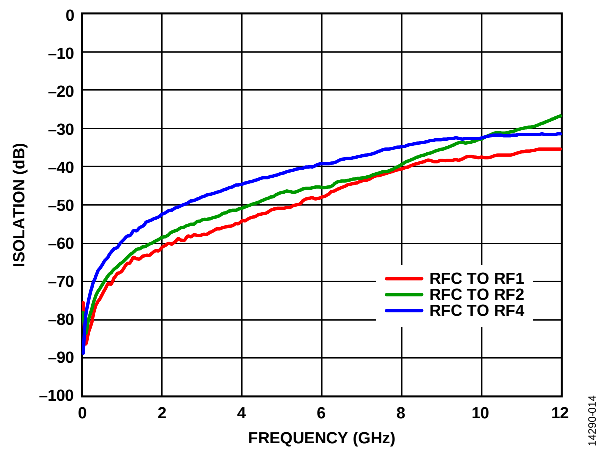


Figure 14. Isolation vs Frequency RFC to RF3 = On

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = −3.3 V, T_{CASE} = 25°C, unless otherwise specified.

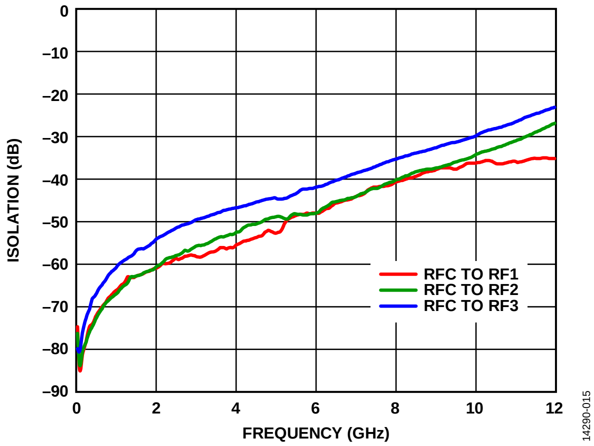


Figure 15. Isolation vs Frequency, RFC to RF4 = On

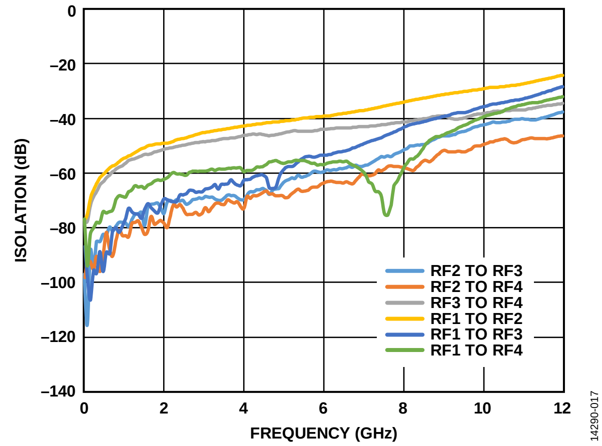


Figure 17. Channel to Channel Isolation vs Frequency, RFC to RF1 = On

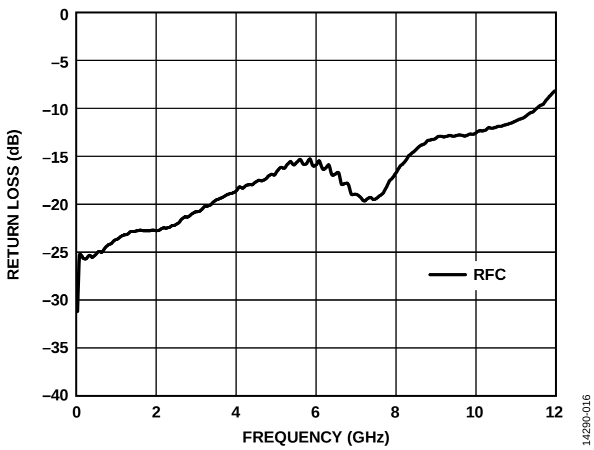


Figure 16. Return Loss vs Frequency, RFC to RF4 = On

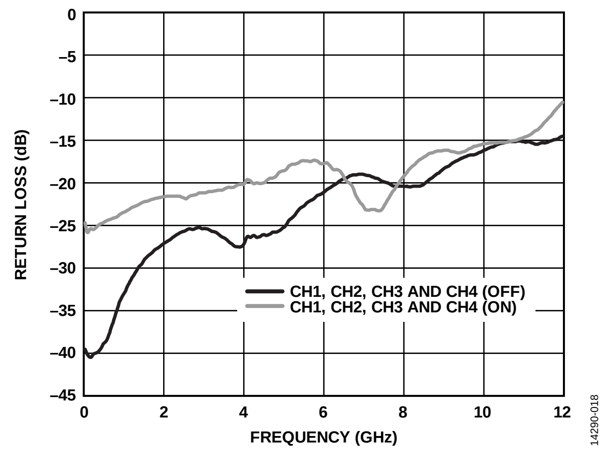


Figure 18. Return Loss vs Frequency, RFC to RF4 = On

INPUT POWER COMPRESSION AND INPUT THIRD-ORDER INTERCEPT

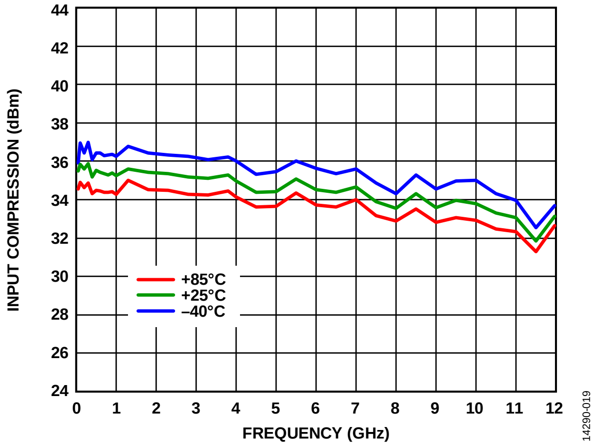


Figure 19. 0.1 dB Compression Point vs Frequency over Temperature, V_{DD} = 3.3 V, V_{SS} = −3.3 V

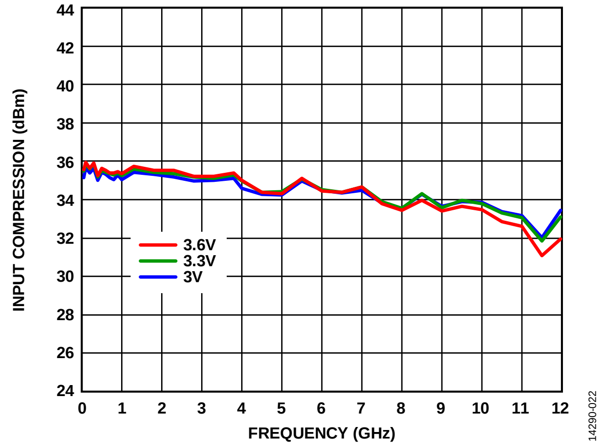


Figure 22. 0.1 dB Compression Point vs Frequency over Voltage T_C = 25°C

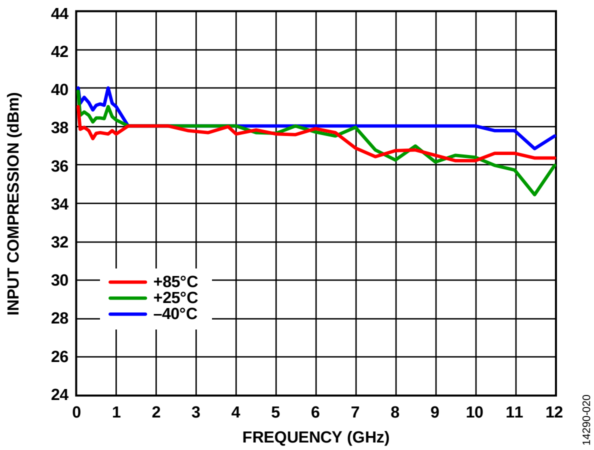


Figure 20. 1 dB Compression Point vs Frequency over Temperature, V_{DD} = 3.3 V, V_{SS} = −3.3 V

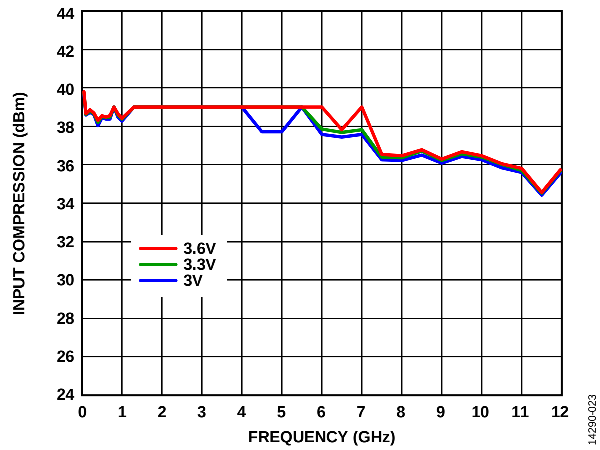


Figure 23. 1dB Compression Point vs Frequency over Voltage, T_C = 25°C

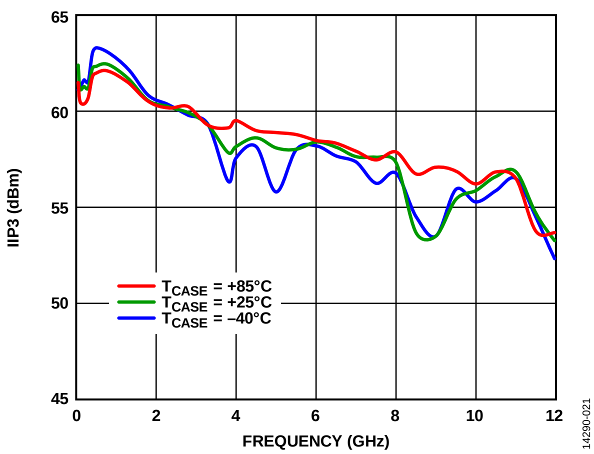


Figure 21. Input Third-Order Intercept (IIP3) Point vs Frequency over Temperature, V_{DD} = 3.3 V, V_{SS} = −3.3 V

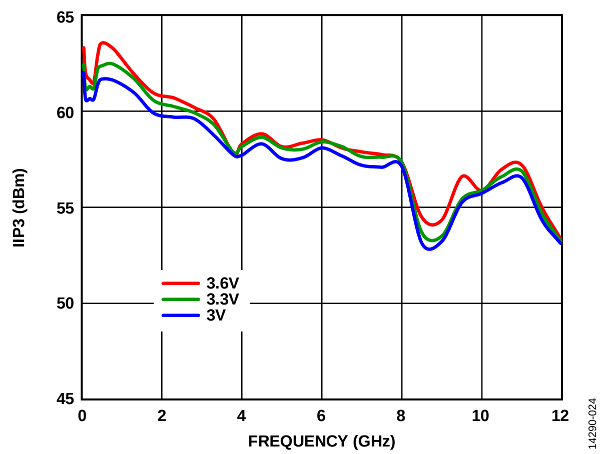


Figure 24. Input Third-Order Intercept (IP3) Point vs Frequency over Voltage, T_C = 25°C

INPUT POWER COMPRESSION AND INPUT THIRD-ORDER INTERCEPT (10 kHz TO 1 GHz)

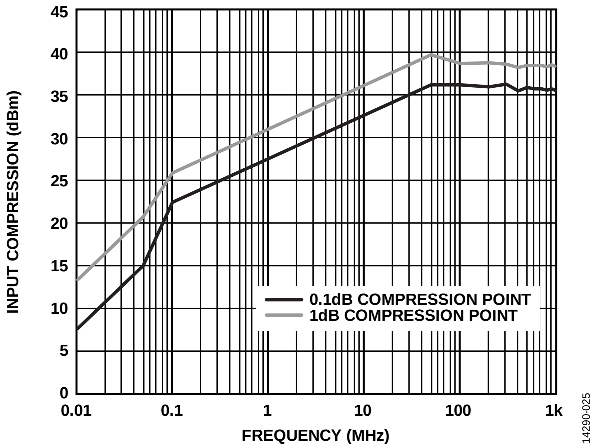


Figure 25. Input Compression Point vs Frequency, V_{DD} = 3.3 V, V_{SS} = −3.3 V at T_C = 25°C

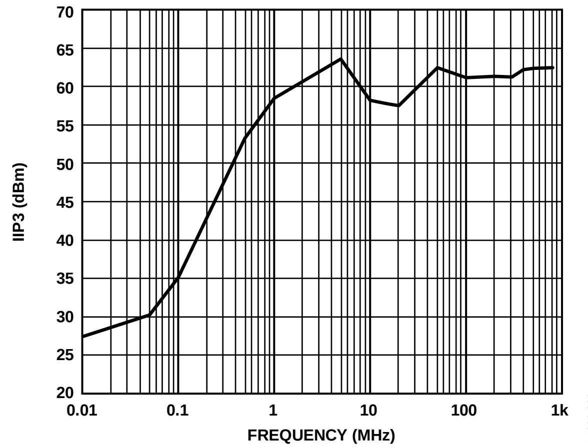


Figure 26. Input Third-Order Intercept (IIP3) Point vs Frequency, V_{DD} = 3.3 V, V_{SS} = −3.3 V at T_C = 25°C

THEORY OF OPERATION

The ADRF5040 requires a positive supply voltage applied to the V_{DD} pin and a negative voltage supply applied to the V_{SS} pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ADRF5040 is controlled via two digital control voltages applied to the V_1 pin and the V_2 pin. A small value bypassing capacitor is recommended on these digital signal lines to improve the RF signal isolation.

The ADRF5040 is internally matched to 50 Ω at the RF input port (RFC) and the RF output ports (RF1, RF2, RF3, and RF4); therefore, no external matching components are required. The RF1 through RF4 pins are dc-coupled, and dc blocking capacitors are required on the RF paths. The design is bidirectional; the input and outputs are interchangeable.

The ADRF5040 does not need any special power up sequencing and relative order to power up V_{DD} and V_{SS} supply is not important. The control signals V_1 and V_2 can be applied a voltage only after V_{DD} is powered-up, in order not to forward bias and damage the internal ESD protection circuits. Also, turn on the RF signal when the device supply settles to a steady state.

APPLICATIONS INFORMATION

EVALUATION PCB

The evaluation PCB shown in Figure 27 is designed using proper RF circuit design techniques. Signal lines at the RF port have 50 Ω impedance, and the package ground leads and backside ground slug must be connected directly to the ground plane. The evaluation PCB is available from Analog Devices, Inc. upon request.

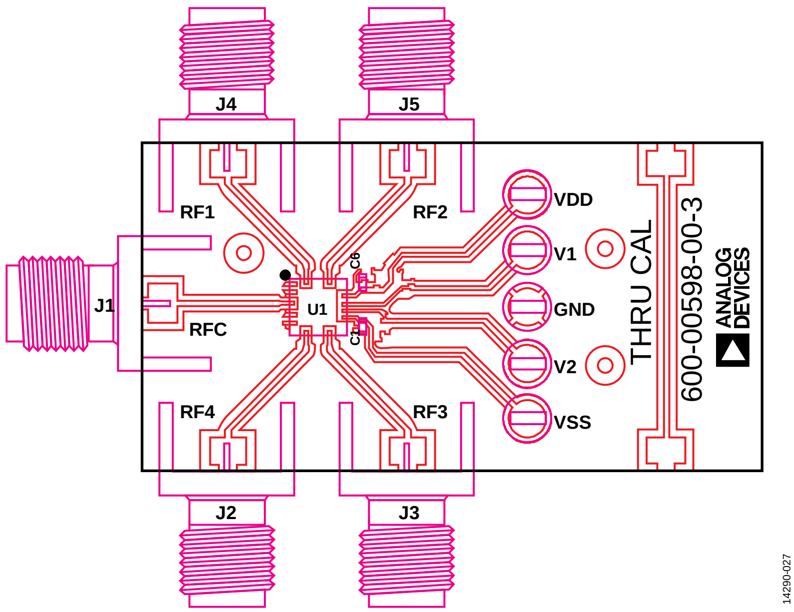


Figure 27. Evaluation PCB

Table 7. Bill of Materials for Evaluation Board ADRF5040-EVALZ

Item	Description
J1 to J5	PC mount SMA RF connectors
TP1 to TP5	Through hole mount test points
C1, C6	100 pF capacitors, 0402 package
U1	ADRF5040 SP4T switch
PCB	600-00598-00-3 evaluation PCB, Rogers 4350 circuit board material

OUTLINE DIMENSIONS

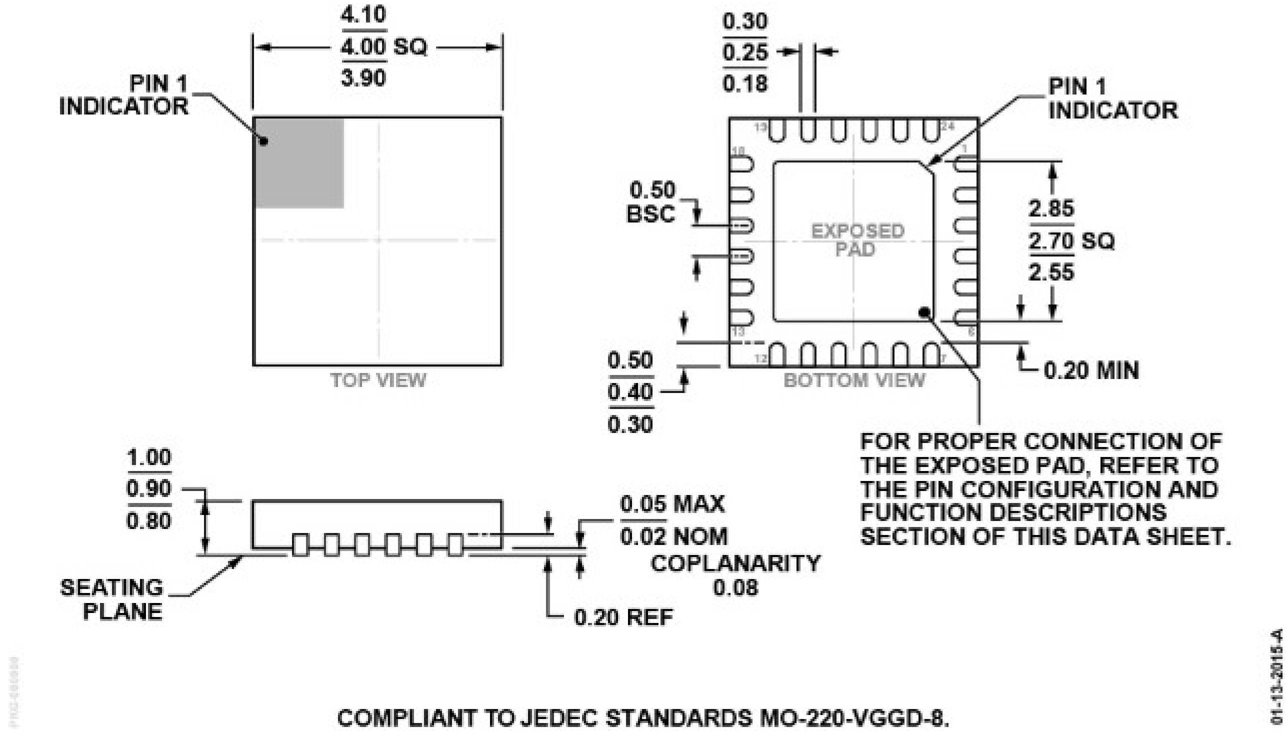


Figure 28. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-16)
Dimensions shown in millimeters

PR14290-0-5/16(PrB)