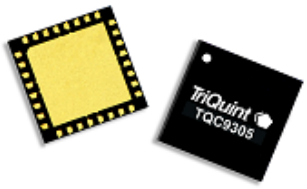
TQC9305

0.7-3.6 GHz Digital Variable Gain Amplifier

Applications

- Wireless Infrastructure
- LTE / WCDMA / CDMA / GSM
- TDD or FDD systems
- General Purpose Wireless

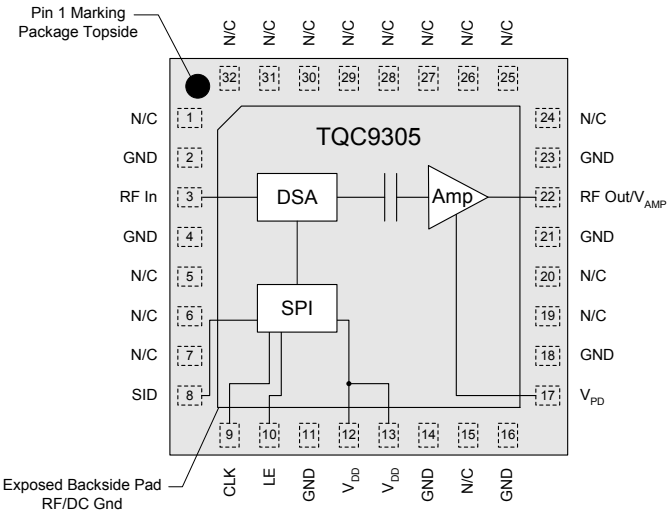


32-pin 5x5mm leadless SMT package

Product Features

- Integrates DSA + Amp Functionality
- 0.7 – 3.6 GHz Broadband Performance
- 5-bit control, 31 dB range
- 13 dB Gain at 1.9 GHz
- 3.1 dB Noise Figure at max gain setting
- +23 dBm P1dB
- +27 dBm IIP3, +40 dBm OIP3
- Integrated on-chip matching, 50 ohm in/out
- Integrated shutdown control for TDD compatibility
- +5V Supply Voltage, 3.3V TTL logic compatible

Functional Block Diagram



General Description

The TQC9305 is a digitally controlled variable gain amplifier (DVGA) with a broadband frequency range of 700 to 3600 MHz. The DVGA features high linearity and low noise while providing digital variable gain with a 31 dB of range in 1 dB steps through a serial mode control interface. At 1.9 GHz, the DVGA typically provides 13 dB gain, +40 dBm OIP3, +23 dBm P1dB and 3.1 dB noise figure. This combination of performance parameters makes the DVGA ideal for receiver applications requiring gain control with high IIP3 and low noise figure. In addition, the DVGA integrates a shut-down biasing capability to allow for easy operation for TDD applications.

The TQC9305 integrates a high performance digital step attenuator followed by a high linearity, broadband gain block. Both stages are internally matched to 50 Ohms and do not require any external matching components. The TQC9305 is packaged in a RoHS-compliant, compact 5x5 mm surface-mount leadless package.

Pin Configuration

Pin No.	Label
1, 5, 6, 7, 15, 19, 20, 24-32	N/C
2, 4, 11, 14, 16, 18, 21, 23	GND
3	RF In
8	SID
9	CLK
10	LE
12, 13	V_{DD}
17	V_{PD}
22	RF Out / V_{AMP}
Backside Paddle	RF/DC Ground

Ordering Information

Part No.	Description
TQC9305	0.7-3.6 GHz DVGA
TQC9305-PCB	Evaluation Board

Standard T/R size = 2500 pcs on a 13” reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
RF Input Power, CW, 50Ω, 24 hr, 25°C	+22 dBm
V_{DD}, Power Supply Voltage	-0.3 to +5.5 V
Digital Input Voltage	-0.3 to V_{DD}+0.5 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{AMP}	+4.75	+5	+5.25	V
V_{DD}	+3		+5	V
T_{ch} (for >10^6 hours MTTF)			+190	°C
Case Temperature	-40		+105	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions: T_{LEAD}=+25°C, V_{AMP} = V_{DD} = +5 V

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		700		3600	MHz
Test Frequency			1950		MHz
Gain	Max gain setting	11.5	13	14.5	dB
Gain Control Range			31		dB
Gain Control Step Size			1		dB
Gain Accuracy	700 – 2700 MHz (major states)	± (0.3 + 4% of Atten. Setting)			dB
Input Return Loss			19		dB
Output Return Loss			16.5		dB
Output P1dB			+23		dBm
Output IP3	Pout/tone = 0 dBm, Δf = 1 MHz		+39.7		dBm
Input IP3	Pin/tone = -13 dBm, Δf = 1 MHz	+23.5	+26.7		dBm
Noise Figure	Max gain setting		3.1		dB
Switching Speed	OFF to ON State (50% V_{PD} to 90% RFout)		0.85		µs
	ON to OFF State (50% V_{PD} to 10% RFout)		2.0		µs
Amplifier Shutdown Control, V_{PD}	On state	0		0.4	V
	Off state (Power down)	1.5		V_{DD}	V
Shutdown pin current, I_{PD}	Off state		140		µA
Amplifier Current, I_{AMP} (pin 22)	On state	100	130	160	mA
	Off state (Power down)		3		mA
DSA Current, I_{DD} (pins 12, 13)			1.4		mA
Thermal Resistance (R_{th})	Channel to case		48.3		°C /W

Serial Control Interface

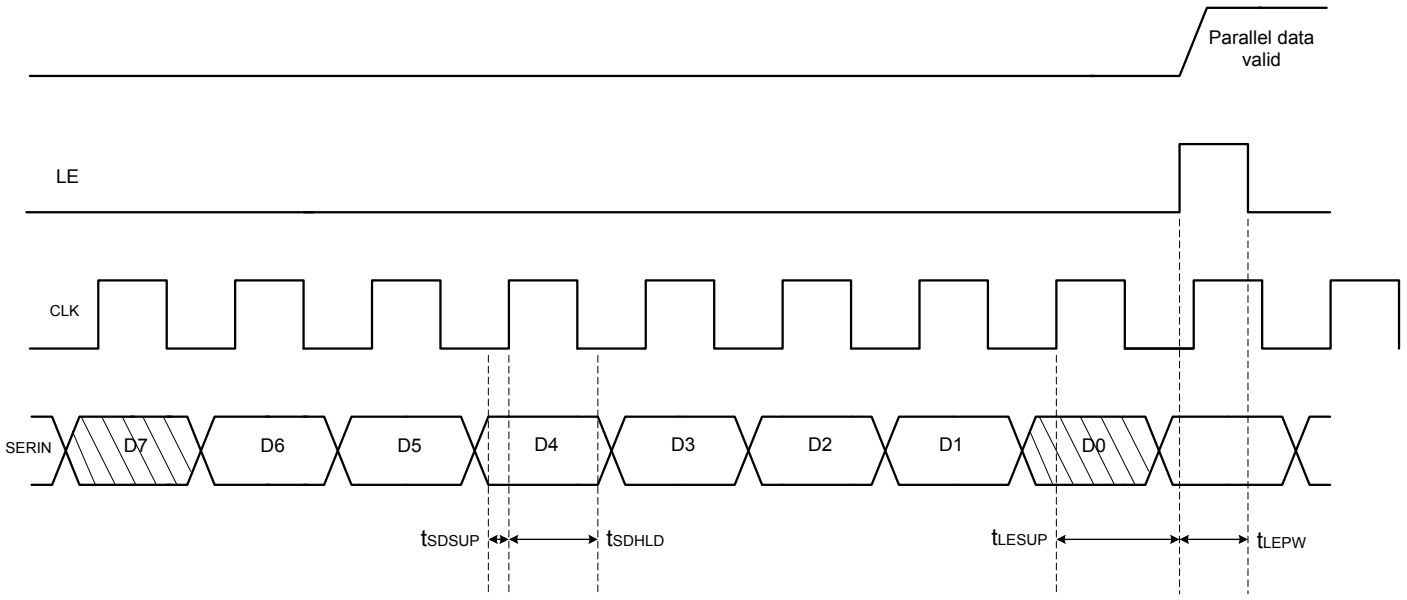
The TQC9305 has a CMOS SPI™ input compatible serial interface. This serial control interface converts the serial data input stream to parallel output word. The input is 3-wire (CLK, LE and SID) SPI™ input compatible. At power up, the serial control interface resets the DVGA to the minimum gain state (maximum attenuation setting). The 8-bit Serial Input Data (SID) word is loaded into the register on rising edge of the CLK, LSB first. When LE is high, CLK is internally disabled in the DVGA.

Serial Control Timing Characteristics (Test conditions: V_{DD} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		20	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	10		ns
LE Pulse Width, t_{LEPW}		16		ns
SID set-up time, t_{SDSUP}	before CLK rising edge	8		ns
SID hold-time, t_{SDHLD}	after CLK rising edge	8		ns
Propagation Delay, t_{PLO}	LE to Parallel output valid	10		ns
LE pulse spacing, t_{LE}	LE to LE pulse spacing	630		ns

Serial Control DC Logic Characteristics (Test conditions: V_{DD} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
Low State Input Voltage, V_{IL}		0	0.8	V
High State Input Voltage, V_{IH}		2.1	V_{DD}	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK	-10	+10	µA



Serial Control Interface

Serial In Control Logic Truth Table, LSB in first

8-Bit Control Word								Attenuation
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	Insertion loss
0	0	0	0	0	1	0	0	1 dB
0	0	0	0	1	0	0	0	2 dB
0	0	0	1	0	0	0	0	4 dB
0	0	1	0	0	0	0	0	8 dB
0	1	0	0	0	0	0	0	16 dB
0	1	1	1	1	1	0	0	31 dB
0	1	0	1	1	0	0	0	22 dB (example)

Note:

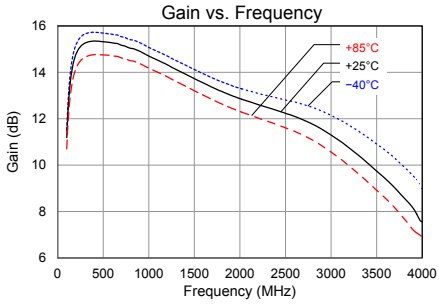
1) Bit D1 needs to be kept logic ‘0’ to maintain the 1dB step for the DSA control.
2) Optionally, the DVGA can be used with a 0.5dB step attenuation by activating bit D1 and hence using 6-Bits (D1-D6).
3) Bits D0 and D7 are ‘don’t care’.

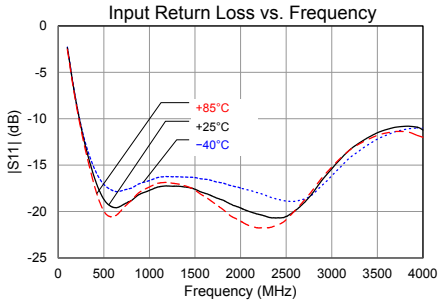
Performance Summary

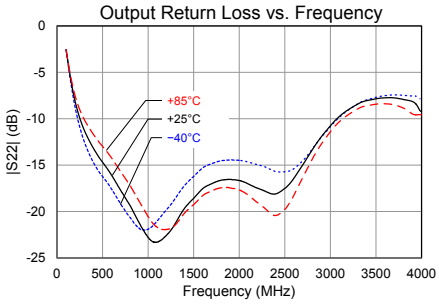
Test conditions: T_{LEAD}=+25°C, V_{AMP} = V_{DD} =+5V, I_{AMP} = 130 mA

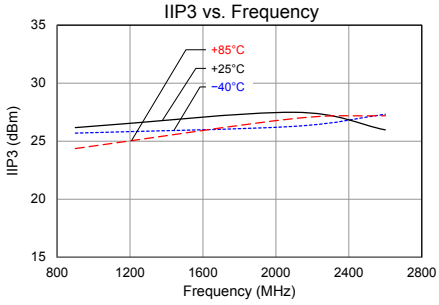
Frequency	900	1700	1950	2140	2600	MHz
Gain	15	13.4	12.9	12.7	12	dB
Input Return Loss	18	18	19	20	18	dB
Output Return Loss	20	17	17	17	17	dB
Output P1dB	+23	+23	+23	+23	+22.1	dBm
Output IP3 (Pout/tone=0dBm, Δf=1MHz)	+41.2	+40	+40	+40	+38	dBm
Input IP3 (Pin/tone=-13dBm, Δf=1MHz)	+26.2	+26.5	+26.7	+27.5	+26	dBm
Noise Figure	2.8	3.0	3.1	3.2	3.6	dB
Amplifier Current, I_{AMP}			130			mA

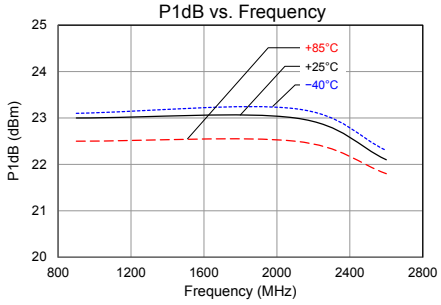
Performance Plots

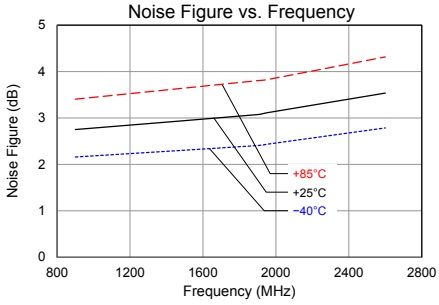


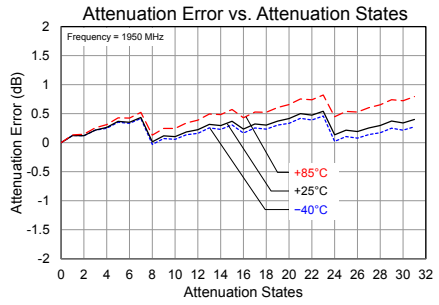


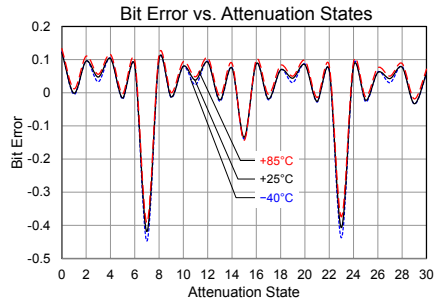


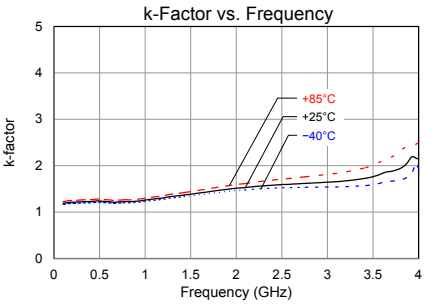




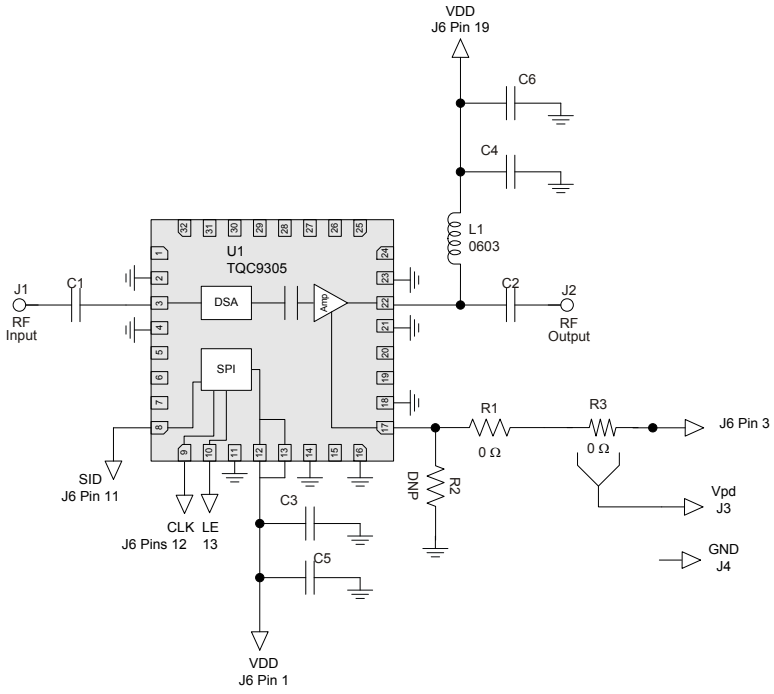


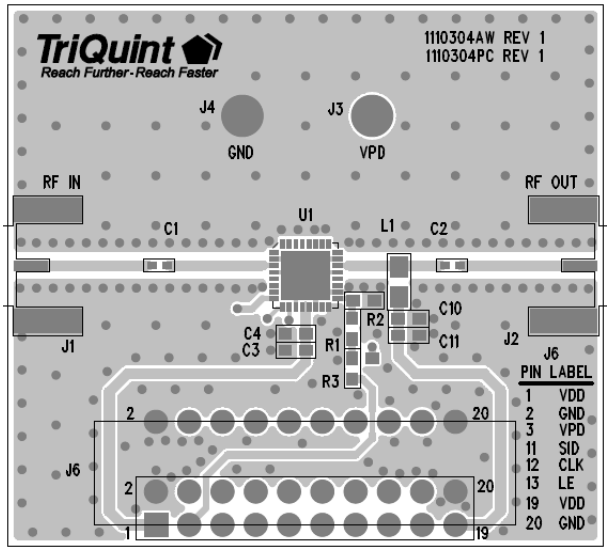






TQC9305-PCB Evaluation Board



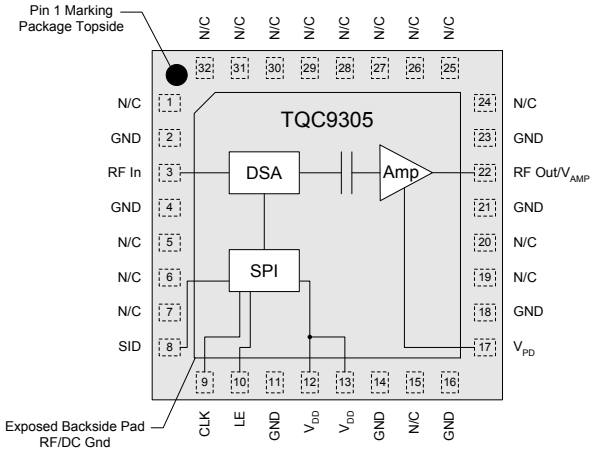


Note: R1, R2 & R3 need not be populated if the shut-down functionality is not required. Pin 17 can be left open or grounded.

Bill of Material: TQC9305-PCB

Reference Desg.	Value	Description	Manufacturer	Part Number
U1	n/a	TQC9305	TriQuint	TQC9305
C1, C2	33 pF	Cap, chip, 0402, 10%, 50V	Various	
C3, C4	100pF	Cap, chip, 0402, 10%, 50V	Various	
C5, C6	1.0uF	Cap, chip, 0603, 10%, 10V	Various	
L1	68nH	Ind, coil, 5%, 0603	Coilcraft	0603CS-68NXJL
R1, R3	0 Ω	Res, chip, 0603, 5%, 1/16W	Various	

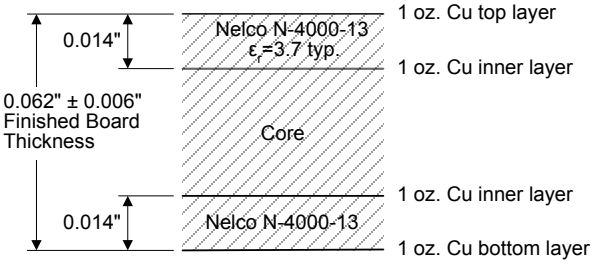
Pin Configuration and Description



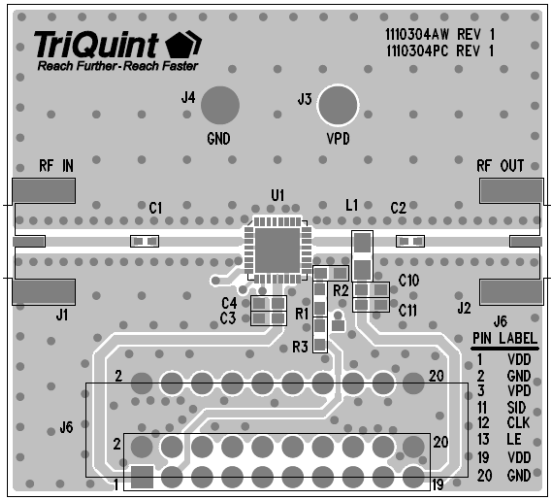
Pin No.	Label	Description
1, 5, 6, 7, 15, 19, 20, 24-32	N/C	No internal connection but can be grounded
2, 4, 11, 14, 16, 18, 21, 23	GND	DC/RF ground connection
3	RF In	RF input. Needs to be capacitively coupled
8	SID	Serial data input
9	CLK	Clock signal in
10	LE	Latch Enable pin
12, 13	V_{DD}	DC Supply Voltage for SPI and DSA. Pins are internally tied together
17	V_{PD}	Amplifier power down control pin
22	RF Out / V_{AMP}	RF output and DC bias for amplifier. Needs to be capacitively coupled
Backside Pad	RF/DC Ground	Ground connection for proper thermal dissipation

Evaluation Board Material Information

TriQuint PCB 1110304 Material and Stack-up



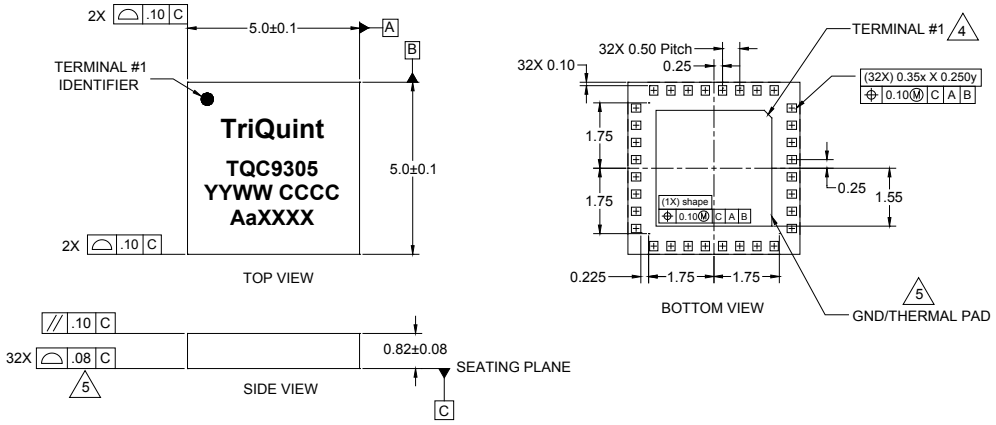
50 ohm line dimensions: width = .026”, spacing = .032”.



Package Marking and Dimensions

Package Marking:

Part number – TQC9305
Year, week - YYWW
Assemblv code - XXXXX

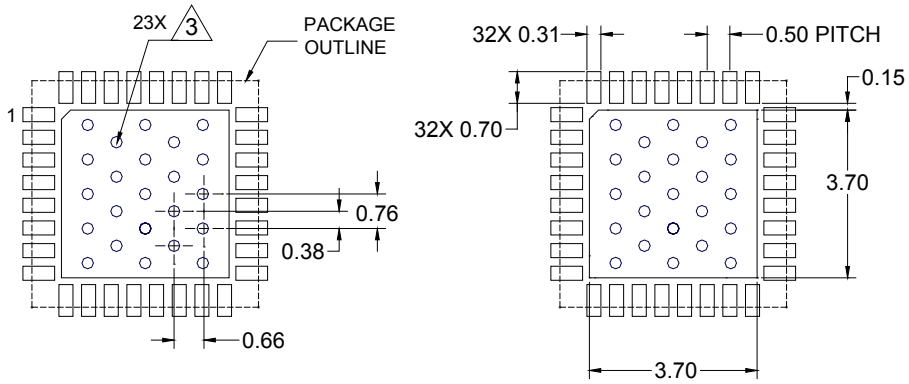


Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-270, Issue B (Variation DAE) for extra thin profile, fine pitch, internal stacking module (ISM).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
5. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.

PCB Mounting Pattern

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating:	Class 1A
Value:	Passes ≥ 250V to < 500V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class C3
Value:	Passes ≥ 1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

MSL Rating:	Level 3
Test:	+260 °C convection reflow
Standard:	JEDEC standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temp.) and tin/lead (245 °C max. reflow temp.) soldering processes.

Package lead plating: Electrolytic plated Au over Ni.

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free
- Lead Free

Contact Information

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